CMOS processing line for heterogenous integration at KTH

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CMOS process line, why?

• Vision
  – Establish a CMOS process technology and design environment available to academic users

• Purpose
  – Benefit research where integration of electronic circuits would add value

• Current objectives:
  – Establish an in-house *reproducible and predictable* CMOS technology
  – Enable the technology in Cadence Virtuoso *design environment* used by circuit designers
Design Rules

**I-line stepper, \( \lambda=365 \text{ nm} \)**

Resolution: 0.5 \( \mu \text{m} \), Alignment: 50 nm

- Active area: width/open 2/2 \( \mu \text{m} \)
- Contact holes (CT): 1x1 \( \mu \text{m}^2 \)
- M1, M2: width/open 2/2 \( \mu \text{m} \)
- M1-CT: overlap 0.5 \( \mu \text{m} \)
- \( L_G = 1 \mu \text{m} \)
- \( W_{PFET}=4 \mu \text{m}, W_{NFET}=2 \mu \text{m} \)

NAND: 16x36 \( \mu \text{m}^2 \)

Die size of 7x7 mm: \( \sim 85 \) kNAND/die

Die size of 21x21 mm: \( \sim 765 \) kNAND/die
Fully Depleted SOI CMOS

1. Alignment mark
2. Si device layer, $t_{Si}=20$ nm
   $5$ nm $SiO_2/12$ nm TiN/100 nm $n^+$-poly-Si
3. Gate mask and etch
4. $n^+$ As impl. 9 keV, $1e15$ cm$^{-2}$
5. $p^+$ BF$_2$ impl. 9keV, $1e15$ cm$^{-2}$
   ALD $SiO_2$/PECVD SiN spacers
   RTA 1000 °C, 10s
6. Silicide block mask
   NiSi formation
   400 nm PECVD SiO$_2$
7. Contact hole mask and etch
   100 nm TiW/500 nm Al
8. Metal 1 mask and etch
   400 nm PECVD SiO$_2$
9. Via hole mask and etch
   100 nm TiW/500 nm Al
10. Metal 2 mask and etch
   10 % H$_2$/N$_2$, 400 °C anneal
Contact chains

Contact process development

<table>
<thead>
<tr>
<th>ETCH: RIE to ENDP</th>
<th>Yield [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resist strip: O₂ plasma</td>
<td>&lt; 1%</td>
</tr>
<tr>
<td>DEP: TiW/Al</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ETCH: RIE to or close to ENDP</th>
<th>Yield [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resist strip: O₂ plasma</td>
<td>&lt; 70%</td>
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<tr>
<td>CLEAN: 1 % HF</td>
<td></td>
</tr>
<tr>
<td>DEP: Ar⁺ sputtering + TiW/Al</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>ETCH: RIE on time</th>
<th>Yield [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 nm &lt; t&lt;sub&gt;SiO₂&lt;/sub&gt; &lt; 40 nm left in CT hole</td>
<td>&gt; 95 %</td>
</tr>
<tr>
<td>Resist strip: O₂ plasma</td>
<td></td>
</tr>
<tr>
<td>CLEAN: 1 % HF 1 min</td>
<td></td>
</tr>
<tr>
<td>DEP: TiW/Al</td>
<td></td>
</tr>
</tbody>
</table>
HF Spray etching

Process established Nov 2015
NFET and PFET electrical characteristics

L=1 µm
W=2 µm

\( \Delta V_T \approx 1 \text{ V} \)

\( \Delta I_{DS} \approx > 10 \times \)

SS \approx 60 - 120 mV/dec.
$I_D = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}}{2} \right)V_{DS}$
Long channel mobility

![Graph showing mobility vs. Ninv]

- **NFET**
  - Esseni et al., IEDM 2001

- **PFET**
  - Esseni et al., IEDM 2000
$V_T$ variability

All devices have TiN deposited by PVD (magnetron sputtering).
ALD TiN, $TiCl_4$, $NH_3$, $T_{dep}=425 \, ^\circ C$
Summary CMOS Process Development

1. Contact hole etch and Metal 1 dep
2. No silicide
3. ALD TiN \((T_{\text{dep}} = 425 \, ^\circ\text{C})\) as gate electrode
4. Calibrate RTA, improved uniformity at \(T=1000 \, ^\circ\text{C}\)
Device characteristics

Before process development

L = 1 µm
W = 2 µm
SS < 70 mV/dec

NSFET
σ = 17 mV

PFET
σ = 13 mV
Transfer characteristics

\[ I_{DS} \text{ [μA/μm]} = \begin{cases} 22 \text{ μA/μm} & \text{for PFET} \\ 107 \text{ μA/μm} & \text{for NFET} \end{cases} \]

\[ \tau_p = \frac{CV}{I_{eff}} = 565 \text{ ps} \]

\[ \tau_n = \frac{CV}{I_{eff}} = 116 \text{ ps} \]
87 stage Ring Oscillator (176 FETs)

\[ f_{RO} = 19 \, MHz \rightarrow \tau = 305 \, ps \]

\[ \tau = \frac{\tau_p + \tau_n}{2} = \frac{565 + 116}{2} = 340 \, ps \]
Comparision with commercial CMOS
Inverter

\[ W_{PFET} = 4 \text{ \(\mu\)m} \]
\[ W_{NFET} = 2 \text{ \(\mu\)m} \]
D-Flip-Flop (26 FETs)
Frequency divider (8 DFF, 212 FETs)

Input frequency = 1 MHz
Input period = 1 µs

T = 256 µs, f = 3.9 kHz
FD SOI CMOS with M3

1. Alignment mark
2. Si device layer, $t_{Si}=20$ nm
   $5$ nm $SiO_2$/$12$ nm TiN/$100$ nm $n^+$-poly-Si
3. Gate mask and etch
4. $n^+$ As impl. $9$ keV, $1e15$ cm$^{-2}$
5. $p^+$ BF$_2$ impl. $9$keV, $1e15$ cm$^{-2}$
   ALD $SiO_2$/PECVD SiN spacer
   RTA $1000$ °C, 10s
   $400$ nm PECVD $SiO_2$
6. Contact hole mask and etch
   Metal 1 deposition
7. Metal 1 mask and etch
   PECVD $SiO_2$ + CMP
8. Via1 hole mask and etch
   Metal 2 deposition
9. Metal 2 mask and etch
   PECVD $SiO_2$ + CMP
10. Via2 hole mask and etch
    Metal 3 deposition
11. Metal 3 mask and etch
    PECVD $SiO_2$ + CMP
12. Pad mask and etch
    $10$ % $H_2/N_2$, $400$ °C anneal

Oxide CMP based metallization
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Design Environment

3 input NAND schematic

PFETs

NFETs

3 input NAND symbol

[@instanceName]

[@partName]
DFF with Set/Reset

Design Rule Check (DRC)
Layout vs. Schematic (LVS)

Process Design Kit (KTH FD SOI)
- Design rules (layers, min width, min distance....)
- Parametrized MOSFETs
- Calibrated transistor model (UTSOI from Leti)
- Post layout extraction of parasitic R,C,L
Calibrated UTSoI model (Leti)

PFETs, L=1 μm, W=2 μm, $V_{DS} = -0.1$V

NFETs, L=1 μm, W=2 μm, $V_{DS} = 0.1$V

Model predicts 87-stage Ring Oscillator frequency of 22 MHz ($f_{\text{meas.}} = 15$-19 MHz)
Digital Cell Library

Digital Cells

AND
NAND, 3NAND
OR
NOR
INV, INV_3x, INV_9x
XOR
BUF, BUF_3x, BUF_9x
BUF_TriState
MUX 2:1, MUX 4:1
DFF, DFF_SR

MUX 4:1

NAND
XOR
INV 9x
NOR
BUF 3x

34 µm
16 µm
## IO Cell Library

<table>
<thead>
<tr>
<th>I/O Cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog_IO</td>
</tr>
<tr>
<td>Analog_IO_ESD</td>
</tr>
<tr>
<td>Digital_Input</td>
</tr>
<tr>
<td>Digital_Input_ESD</td>
</tr>
<tr>
<td>Digital_Output</td>
</tr>
<tr>
<td>Digital_Output_ESD</td>
</tr>
<tr>
<td>VDD</td>
</tr>
<tr>
<td>VSS</td>
</tr>
</tbody>
</table>

Drive off chip capacitance = 20 pF at $t_{\text{rise}} \sim 1$ ns

Digital Output

- 100 µm
- 200 µm
Work in progress….

- Adjust $V_T$ of PFET and NFET $+0.15$ V to achieve symmetric $V_T$
- Reduce access resistance $R_{SD}$ of NFET
- Improve calibration of UTSOI model
- Evaluate $V_T$ variability of matched devices for analog circuits
- Evaluate antenna effect and incorporate rule in DRC
- Evaluate power consumption and timing
CMOS technology and circuits for heterogeneous integration

Goal:
- **establish a reliable CMOS technology** at KTH with necessary infrastructure to go from commonly used **Electronic Design Automation** environment to **fabricated wafers** in the myfab node **Electrum Laboratory**.

- provide academic **researchers** access to a **CMOS technology** that can be **adapted** to enable **integration with non-conventional devices** (e.g. biosensors, chemical sensors, energy harvester, optical components...) and thus enable research projects to exploit the benefits that on wafer integration with electronics can provide.

Project time: 2019-2021

Year 1: Establish technology and process design kit
Year 2 and 3: Collaborate with researchers and execute heterogenous integration with CMOS
Example: Chemical sensor

- 32 individual sensors
- 5 to 32 binary decoder
- Inkjet printing on sensor areas
Thanks to those who is doing the work....

Current and former PhD students

All M.Sc. students in the course Nanofabrication at KTH

Staff at Division of Electronics:

Staff at Electrum Laboratory

Thanks to those who is paying the work....
Collaborate on heterogenous integration with CMOS?

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