Chemical Mechanical Polishing

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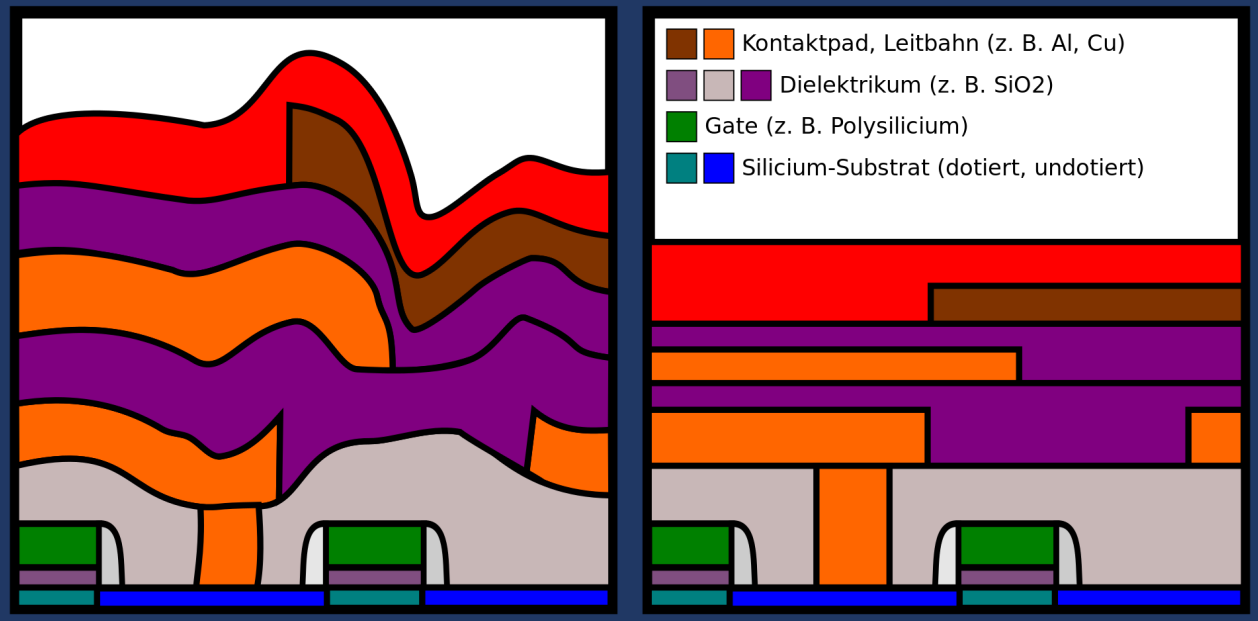
KTH – EECS

Outline

- **Purpose**
- Technology
- CMP Basics
- IPEC/Axus Avanti 472

What can we achieve with CMP?



Without CMP

With CMP

https://de.wikipedia.org/wiki/Chemisch-mechanisches_Polieren#/media/File:Semiconductor_fabrication_with_and_without_CMP_DE.svg

Definition of Planarization

- **Planarization** is a process that removes the surface topologies, smoothens and flattens the surface
- The **degree** of planarization indicates the flatness and the smoothness of the surface

Global planarization

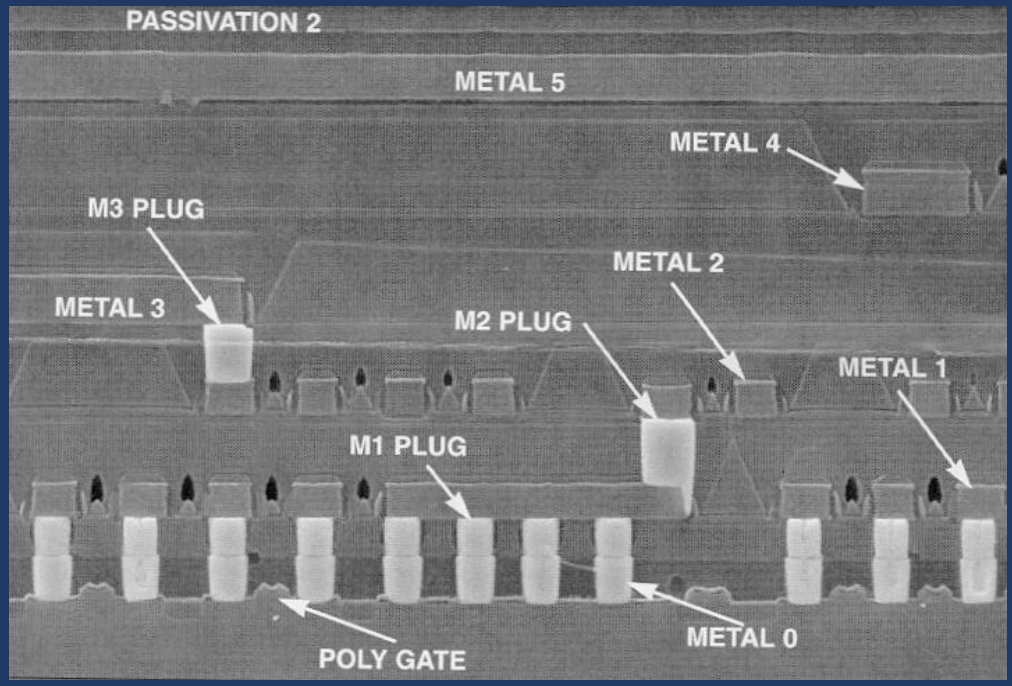
Necessity of CMP

- 0.25 µm pattern require **roughness < 200 nm**, only CMP can achieve this planarization
- When feature size > ~ 0.5 µm, other methods can be used

- Planarized surface allows higher resolution of **photolithography** process
- The planarized surface eliminates **sidewall thinning** because of poor PVD step coverage

Applications of CMP

- **Dielectric** layer planarization
- **Metal** interconnection
- Wafer **bonding**
- Layer **polishing**



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- **Technology**
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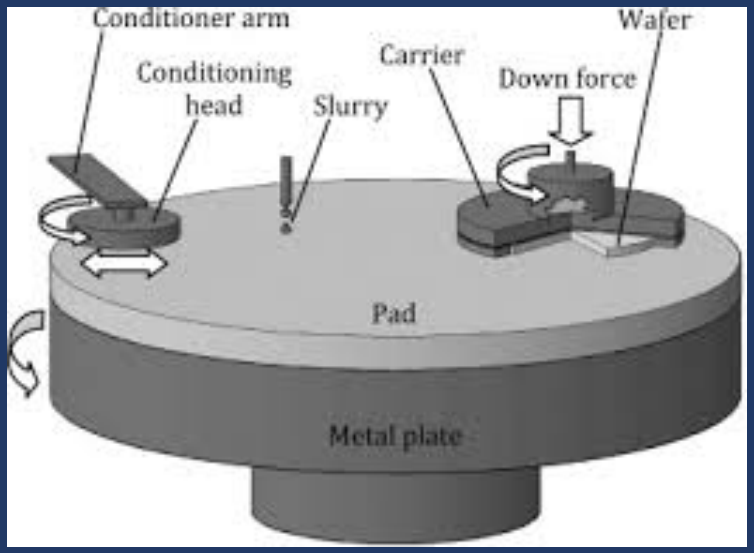
Technology



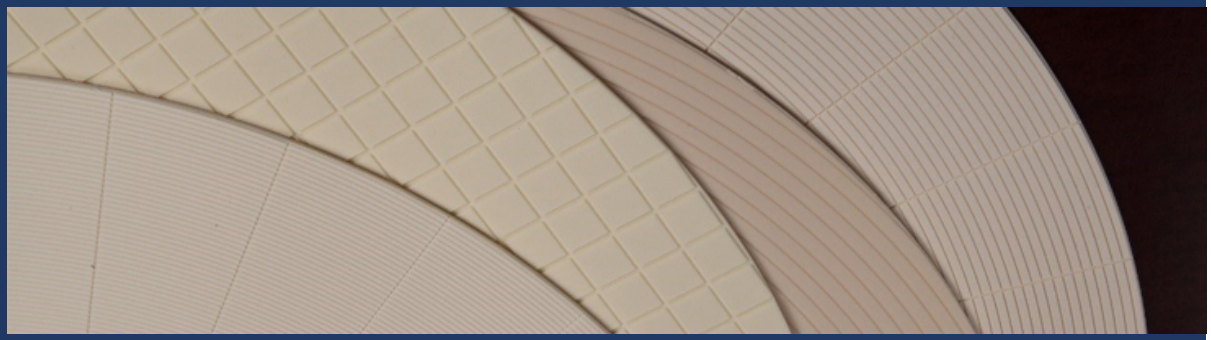
Main components:

- Wafer carrier
- Slurry
- Polishing pad

https://globallup.com/wp-content/uploads/2019/02/Chemical-Mechanical-Polishing-CMP-Diamond-Pad-Conditioner.jpg

Polishing pad

- Material **hardness**
  - Hard → better WIDU
  - Soft → better WIWU
- Pad **roughness**
  - Smoother → < selectivity
  - Rougher → better planarization
- **Conditioning** resurfaces the pad



WIDU: within die uniformity
WIWU: within wafer uniformity

http://www.dupont.com/content/dam/Dupont2.0/Products/Electronics-and-imaging/images/Textimages/cmp-pads-header.jpg

Slurry

- **Chemical** action
- **Mechanical** grinding

- Oxide: alkaline solution with silica
- Metal: acidic solution with alumina

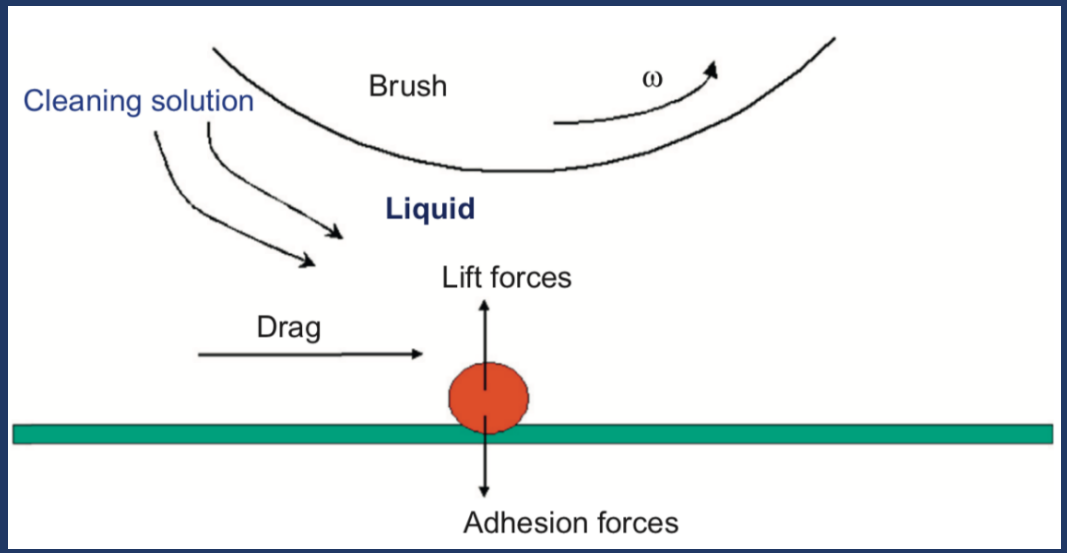
- **Particles size ~100 nm → cleaning** and machine in a specific area of cleanroom

Lee, Dasol & Lee, Hyunseop & Jeong, Haedo. (2016). Slurry components in metal chemical mechanical planarization (CMP) process: A review. International Journal of Precision Engineering and Manufacturing. 17. 1751-1762. 10.1007/s12541-016-0201-y

Post-processing clean

Post-CMP cleaning need remove both particles and other chemical contaminants. Otherwise, higher defect density and lower yield

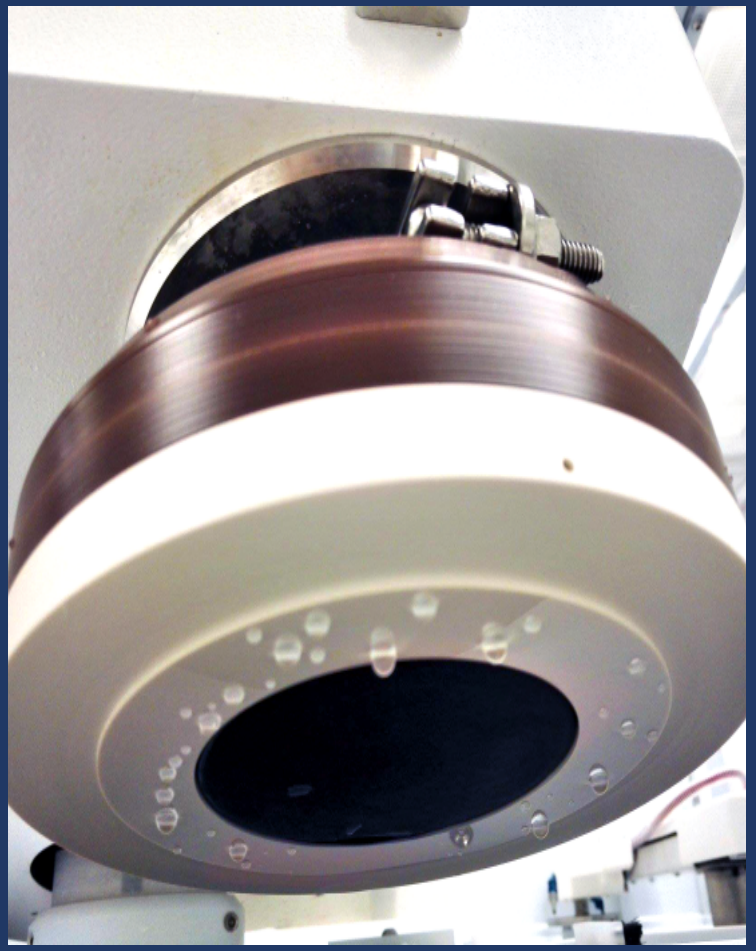
- Batch cleaning (megasonic)
  - DI-H_2O
  - SC-1 (standard cleaning 1)
  - HF/SC-1
  - HF/O_3
- Single wafer cleaning (brush)



Keswani, Manish & Han, Zhenxing. (2015). Chapter 4: Post CMP Cleaning, Developments in Surface Contamination and Cleaning, Volume VIII Wet and Dry Cleaning Methods.

Wafer carrier

- Polishing **uniformity**
- Different **wafer sizes**
- **Direction** of rotation



Outline

- Purpose
- Technology
- **CMP Basics**
- IPEC/Axus Avanti 472

Theory

- **Removal Rate (RR)** discovered and modeled by Preston
  - Direct proportionality to polishing **pressure** and relative **velocity** between pad and wafer
  - Very good approximation for **bulk film** polishing

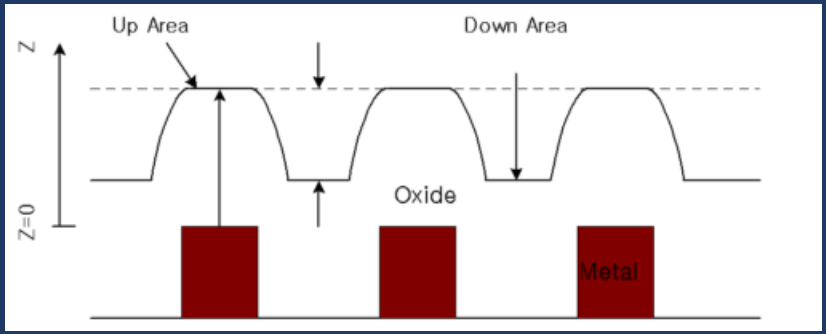
$$RR \propto P, v$$

Theory

- It's possible to estimate the expected **roughness**:
  - Direct proportionality to polishing **pressure** (*P*) and slurry particles **dimension (**Φ**)**
  - Inverse proportionality to **Young** modulus (*E*) of material to be removed

$$R_s \propto \frac{\Phi P}{E}$$

Pattern dependencies



- **Inverse** proportionality between pattern density (PD) and RR
- Pressure decreasing (and RR) as area increasing

To have good uniformity, open areas **filling structures** are needed

$$RR \propto \frac{1}{PD}$$

B. G. Ko, H. C. Yoo, and J. G. Park, "Effects of Pattern Density on CMP Removal Rate and Uniformity," *Measurement*, vol. 39, no. December, pp. 318–321, 2001

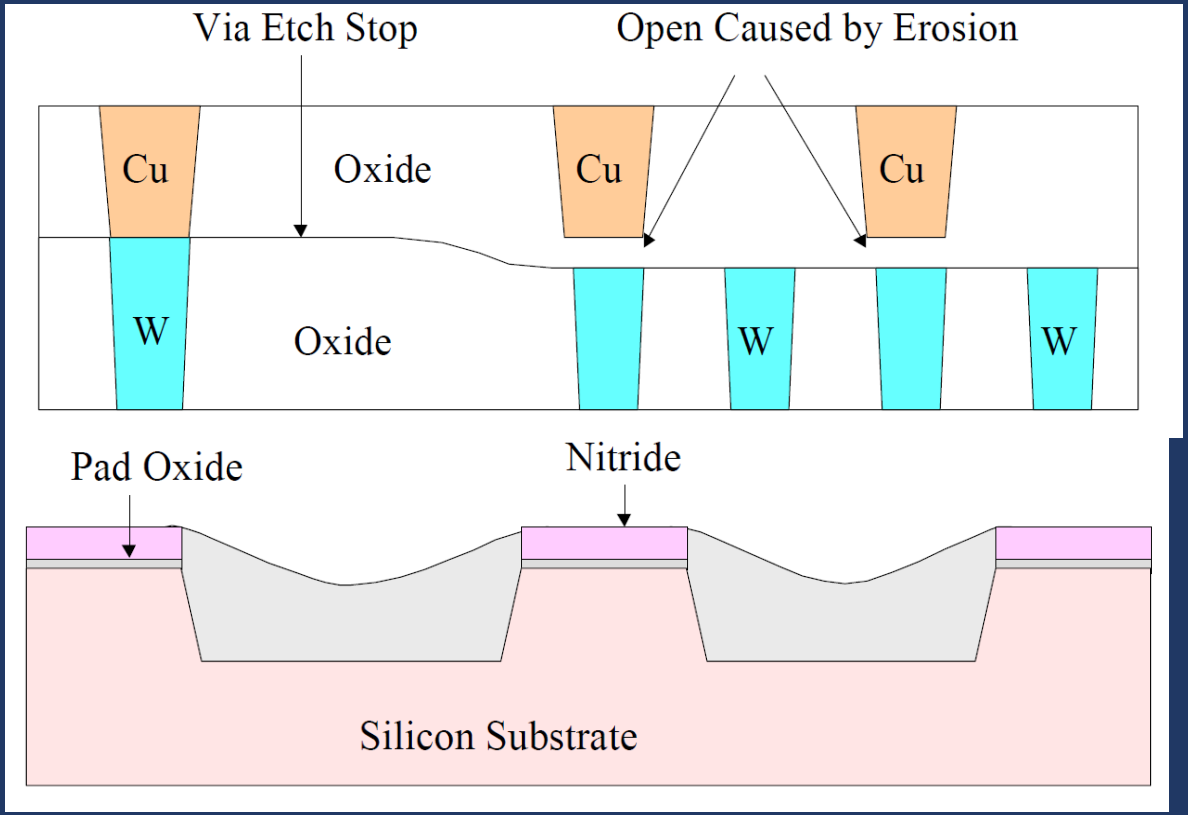
Defects

EROSION

Low selectivity

DISHING

High selectivity



www2.austin.cc.tx.us/HongXiao/Book.htm

Outline

- Purpose
- Technology
- CMP Basics
- **IPEC/Axus Avanti 472**

IPEC/Axus Avanti 472

Wafer **sizes**:

- 50 mm
- 75 mm
- 100 mm
- 150 mm

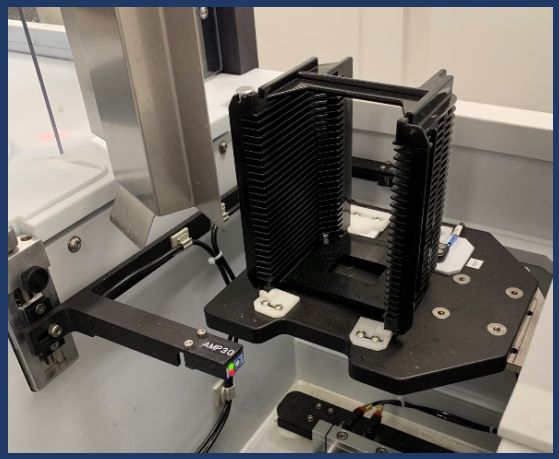
NO PIECES

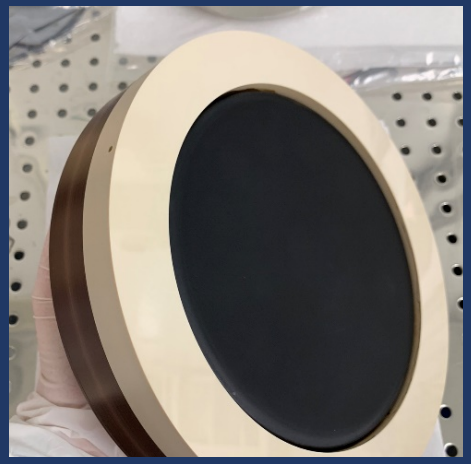
Materials:

- SiO_2
- Si/SiGe
- SiC
- SiN
- InP/GaAs

Features

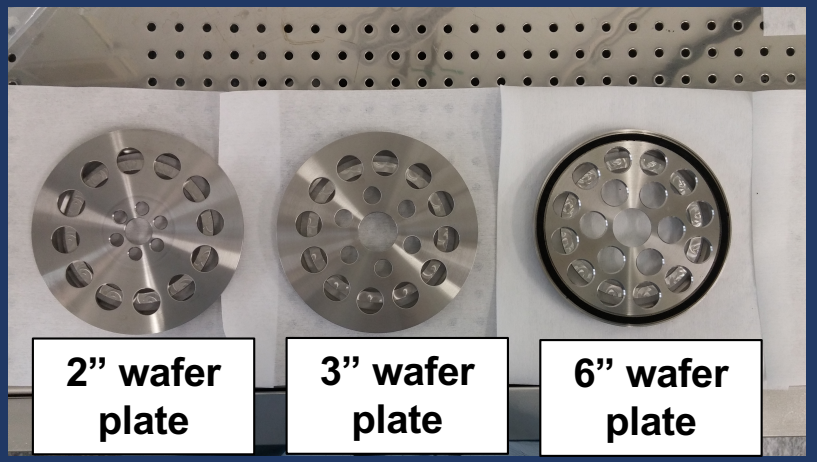
- **Automatic** cassette-to-cassette (100 mm) Si-wafer
- **Titan** carrier
- **2 pads**

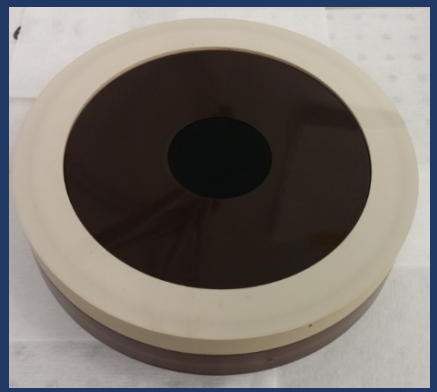


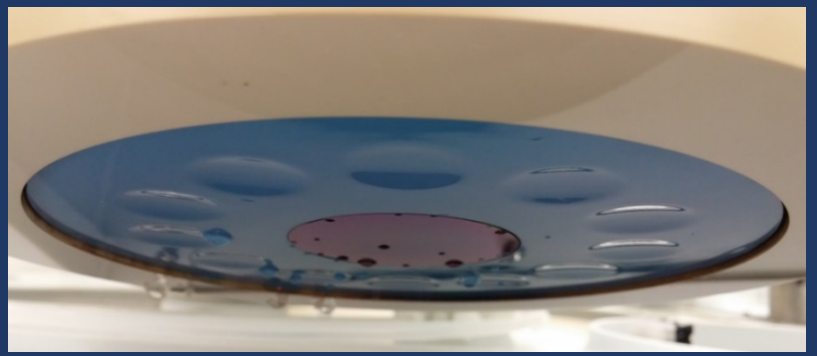


Modifications for carrier head

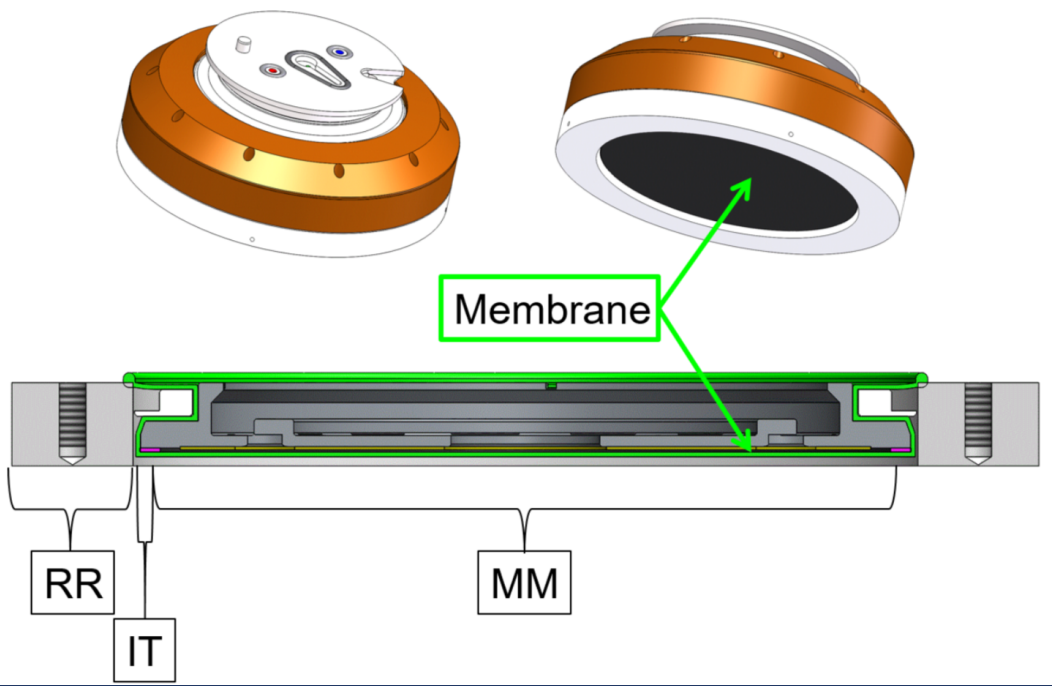
- Adapting the **6” carrier**
- **Different plates** for different wafer diameters
- Additional **inset ring** to keep the wafer in the center of the holder during polishing







Titan™ Carrier Head



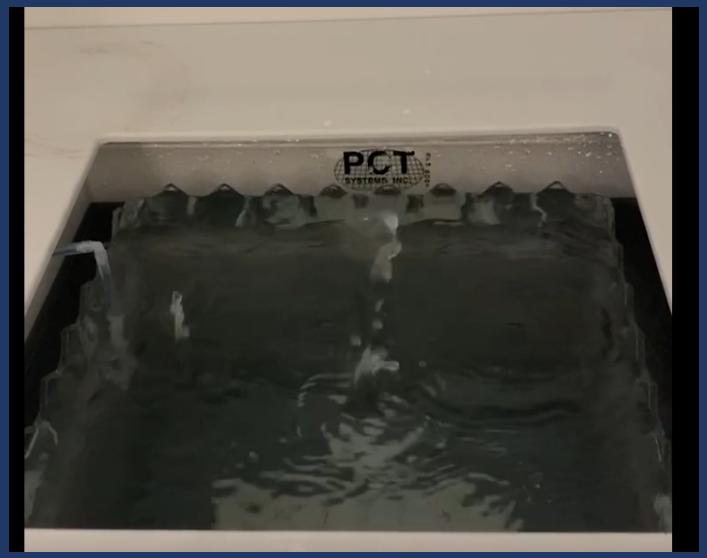
Pressures to optimize process

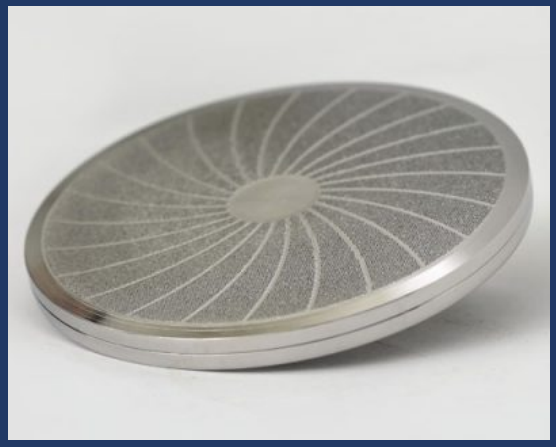
- RR – retainer ring
- MM – membrane pressure
- IT – inner tube

Molines Colomer, R. (2017). Evaluation of Chemical Mechanical Planarization Capability of Titan™ Wafer Carrier on Silicon Oxide.

Features

- **Megasonic** bath – for cleaning
- Primary pad **conditioner**





- All **wet** process
- **Amber** clean
- **SC1** and **SC2**


EMERGENCY
OFF
LOAD SERVICE SWITCH

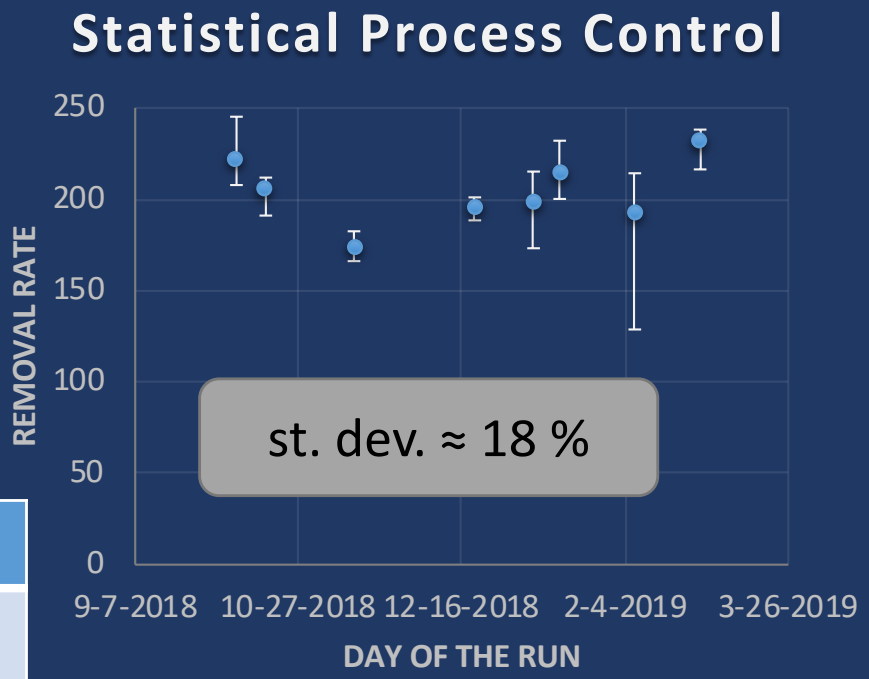
Outline

- Purpose
- Technology
- CMP Basics
- IPEC/Axus Avanti 472
  - **SiO_2**
    - **Metallization**
  - **SiN**
  - **GaAs**
  - **SiC**

SiO_2 PECVD processes

- Polishing rate over months
- Surface roughness
- Wafer to wafer non-uniformity
- Within wafer non-uniformity

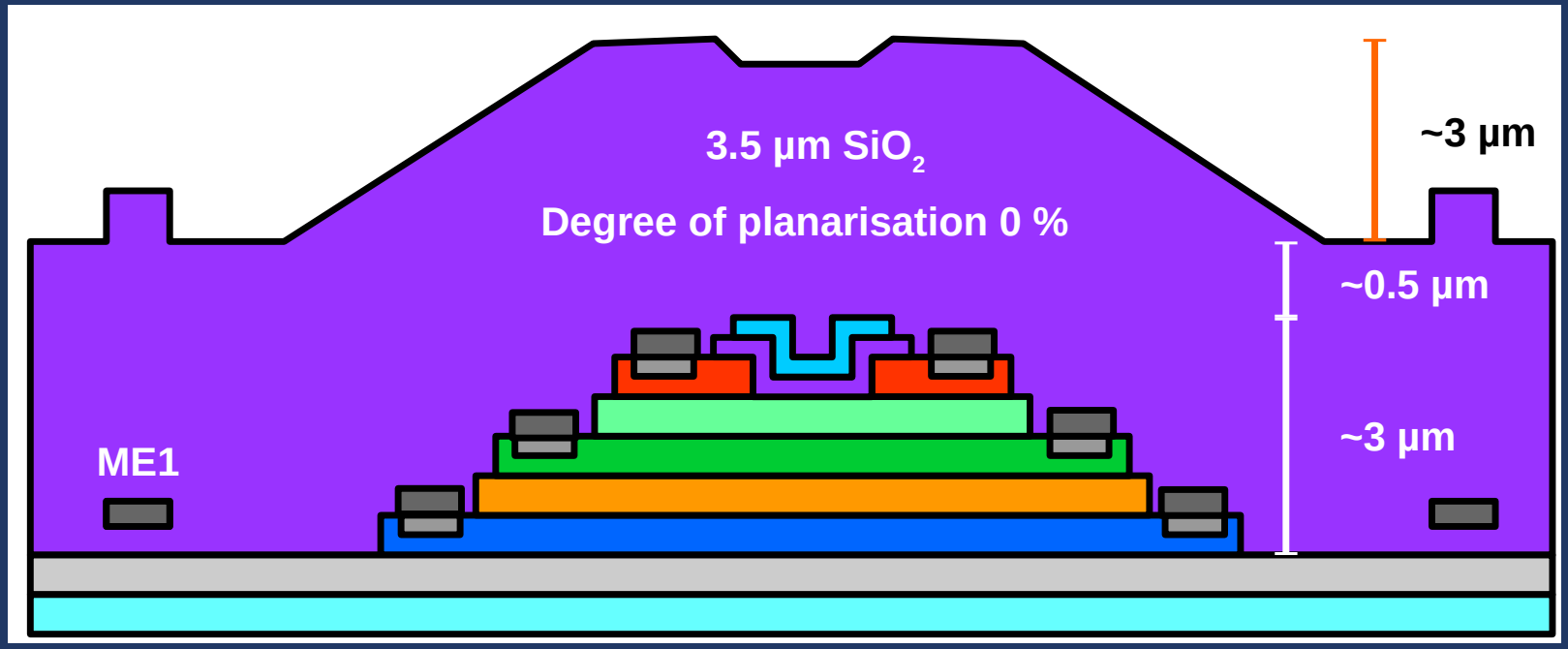
RR	WIWNU	WTWNU	R_s
510 nm/min	3 %	2 %	0.7 nm
230 nm/min	2 %	1 %	0.8 nm
80 nm/min	5 %	5 %	0.3 nm



SLURRY: Cabot SS25E:DIW [1:1]
PAD: Cabot D100 (primary)

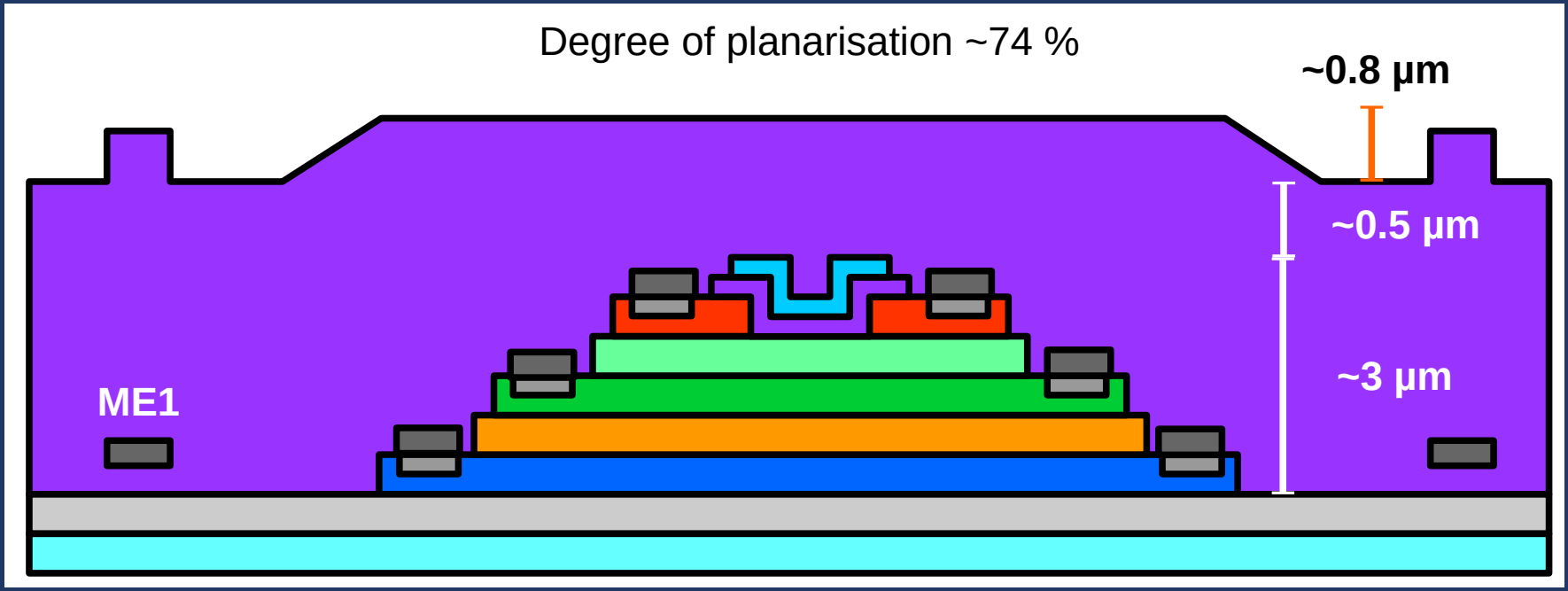
Metallization processes

Starting point



Recessed channel SiC NMOS, lateral dimensions:
166 µm × 112 µm

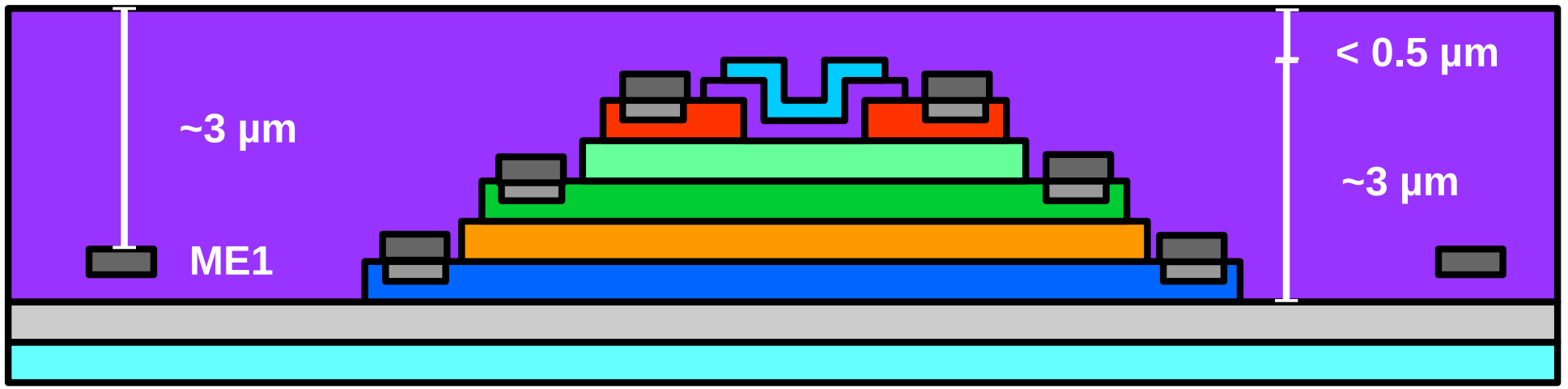
Metallization processes



2 min polishing

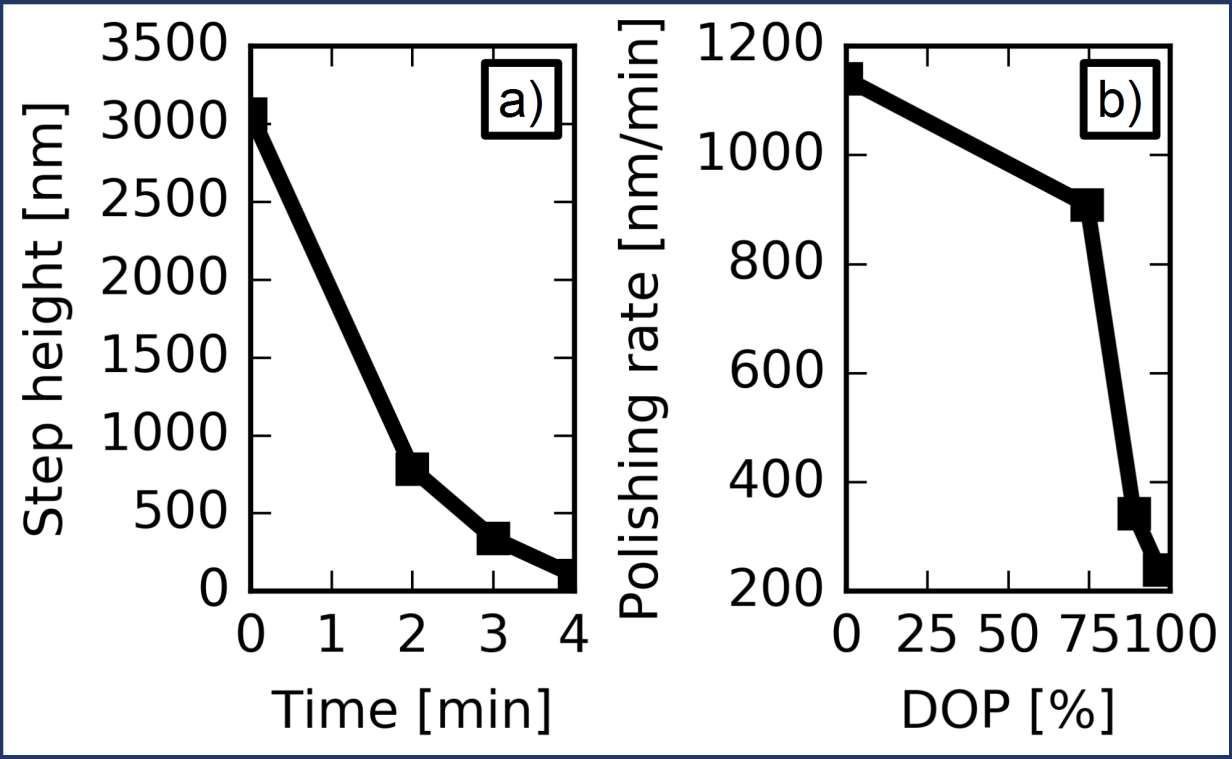
Metallization processes

Degree of planarisation ~97 %



4 min polishing

Metallization – results



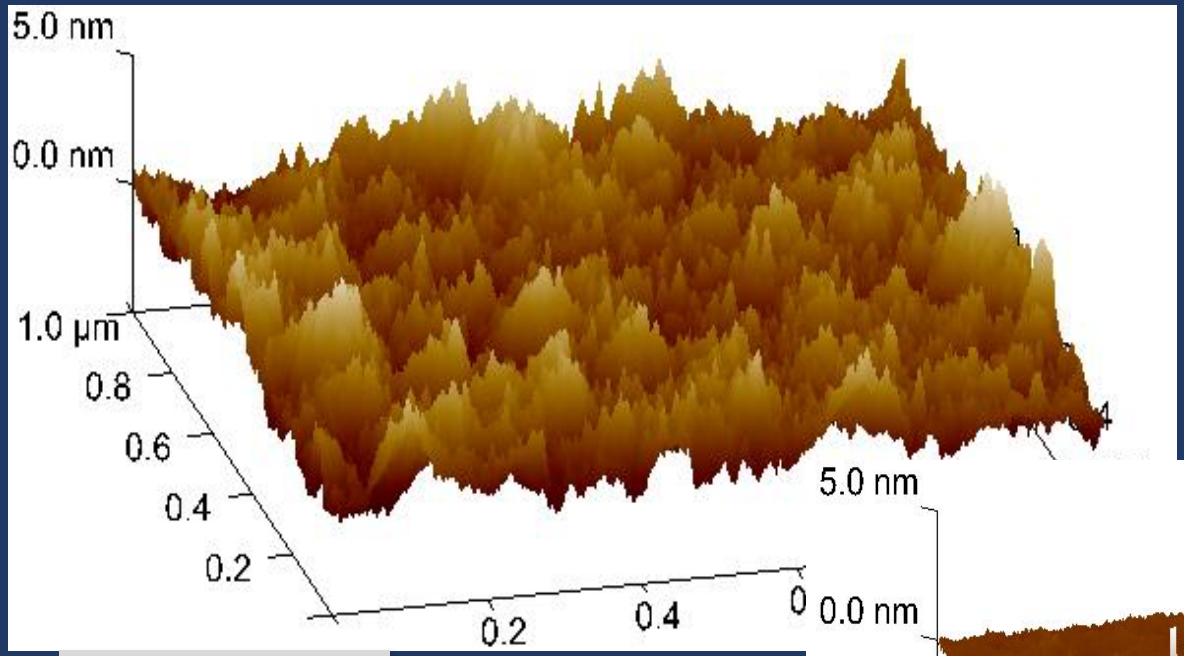
DOP:
Degree of planarisation

0 %: No planarisation
100 %: Perfect planarisation

Planarisation is **self-limiting**
Polishing rate is **pattern dependent**

M. Ekström, SiC CMOS and memory devices for high-temperature integrated circuits, URN: urn:nbn:se:kth:diva-250276

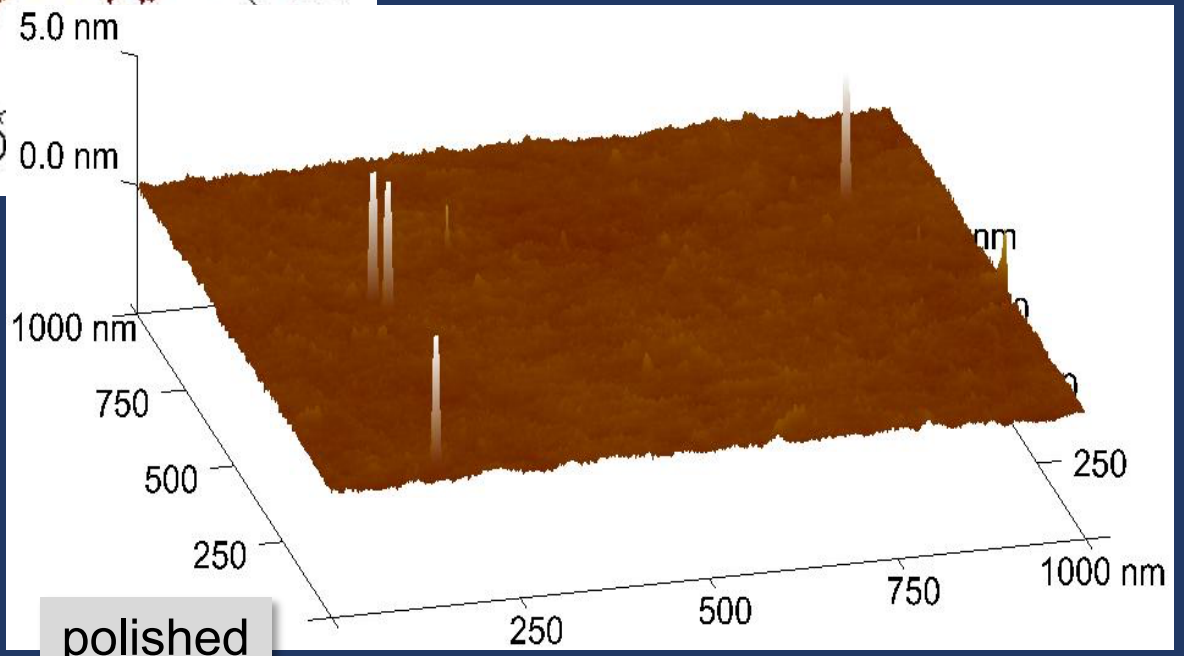
CMP of low-stress LPCVD Si_xN_y



as deposited

PRE R_s	POST R_s
0.89 nm	0.17 nm

RR ≈ 15 nm/min

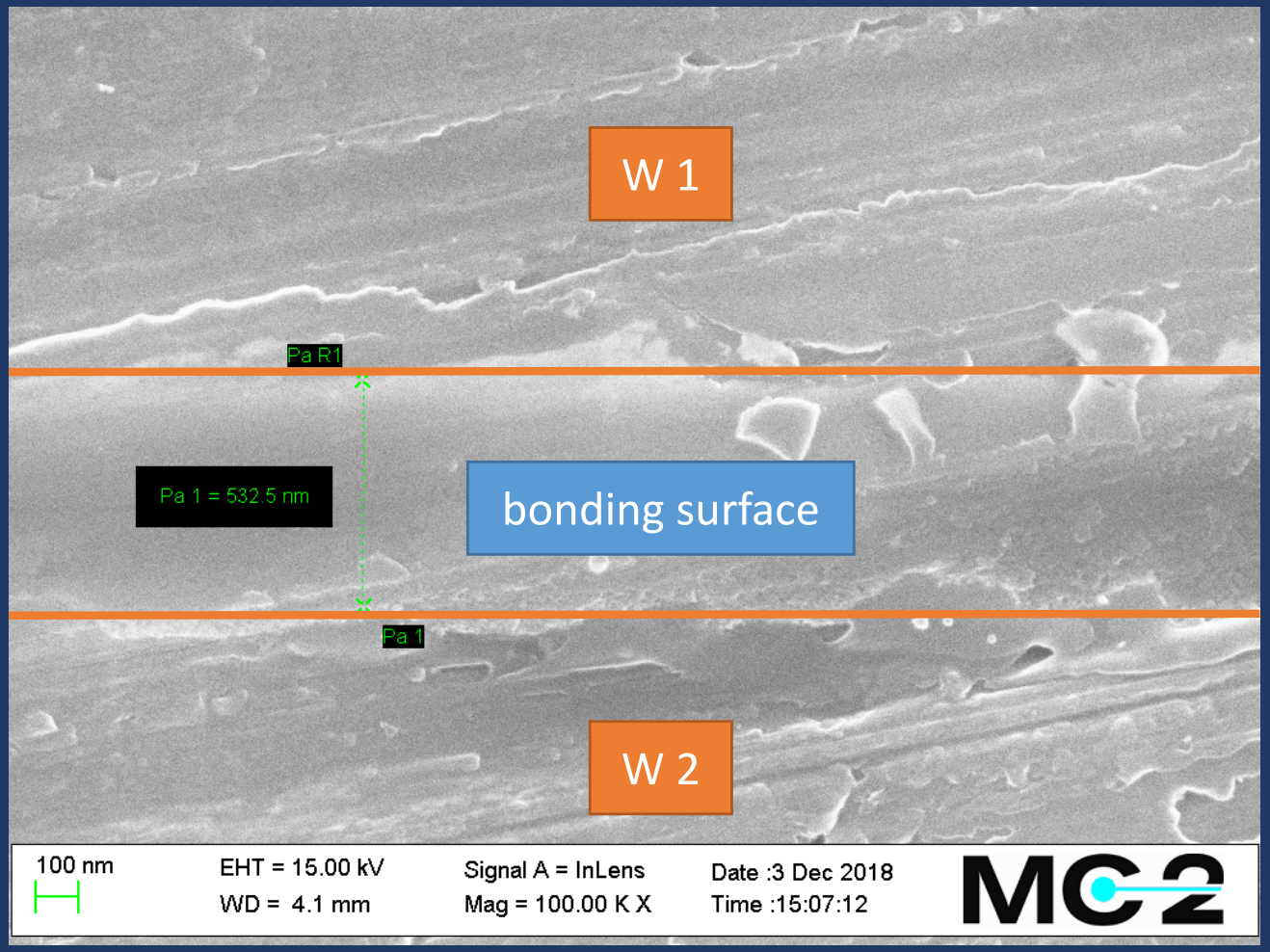


polished

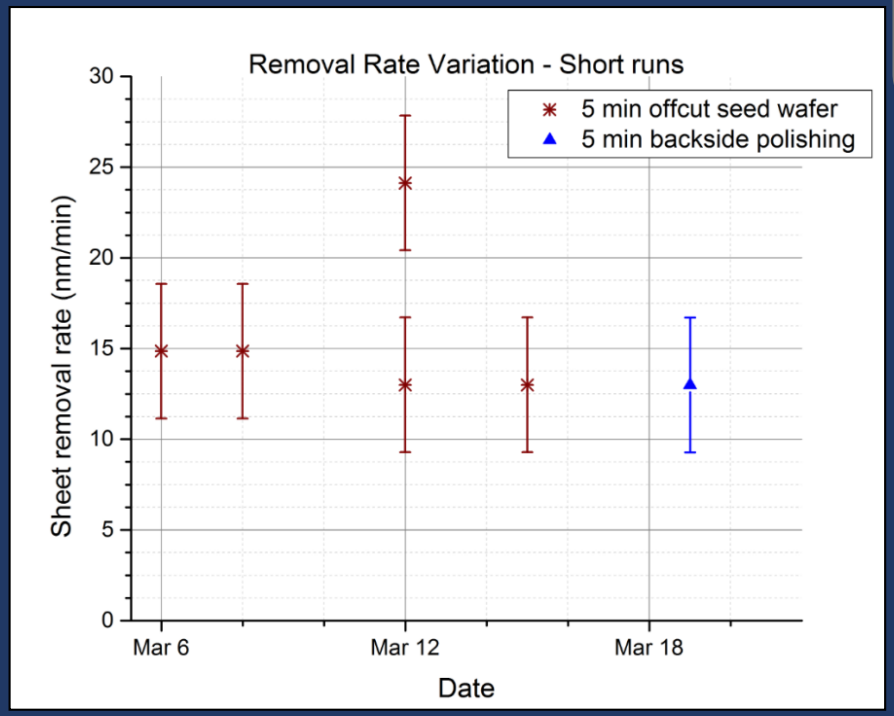
SLURRY: Cabot SS25E:DIW [1:1]
PAD: Cabot D100 (primary)

SiN wafer bonding

SEM image of **fusion bonded** SiN-surfaces



GaAs processes



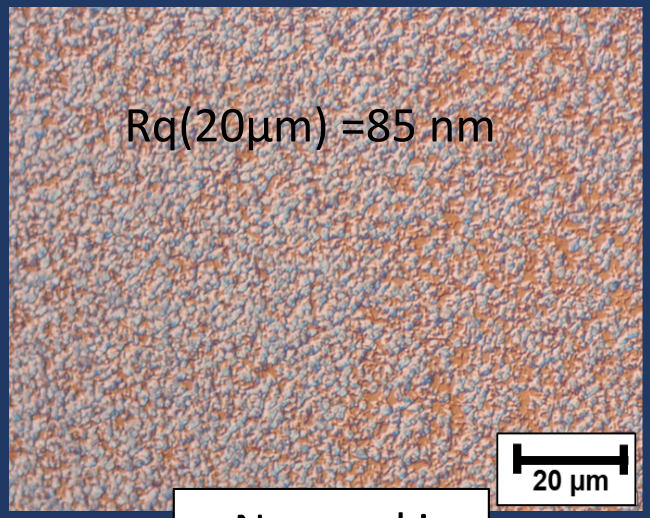
SLURRY: Eminess Ultra-Sol 556:DIW [1:20]
PAD: F TABLE 1 DOW (final)

2” wafer planarization development

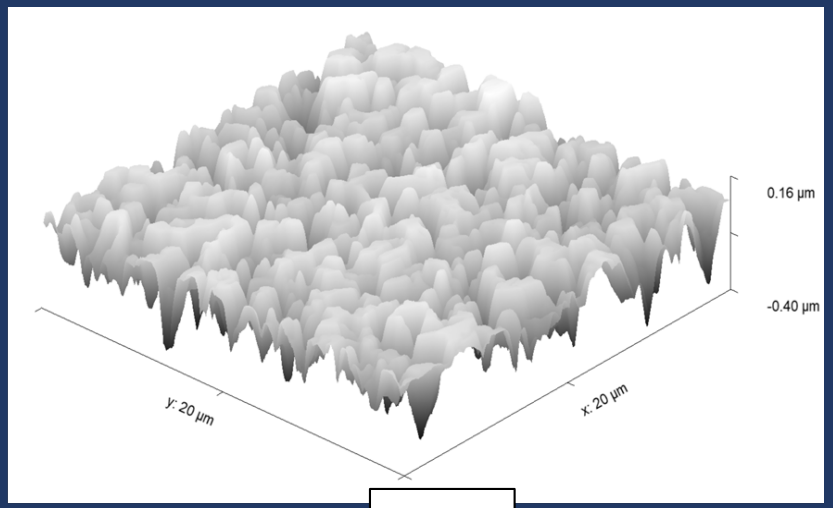
RR = **14±2** nm/min

Removal rate variation for shorter runs, of which 5 are performed on the same wafer. The high uncertainty is due to the low mass-removal.

GaAs planarization

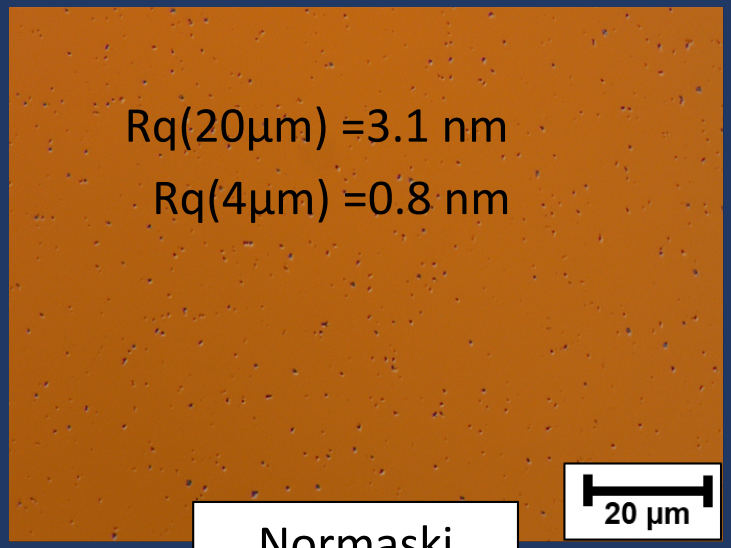


Normaski

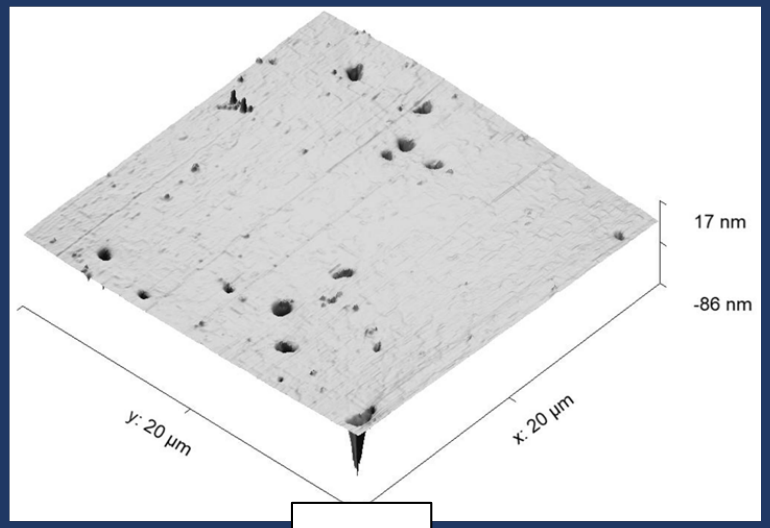


AFM

BEFORE CMP



Normaski



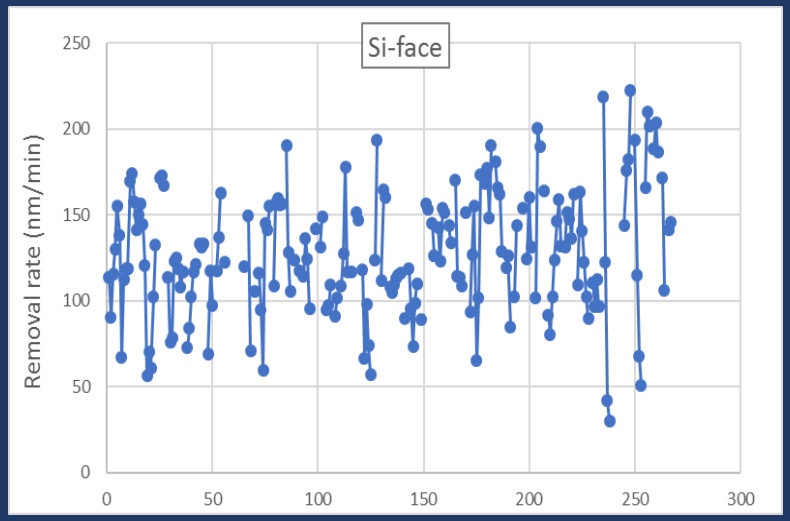
AFM

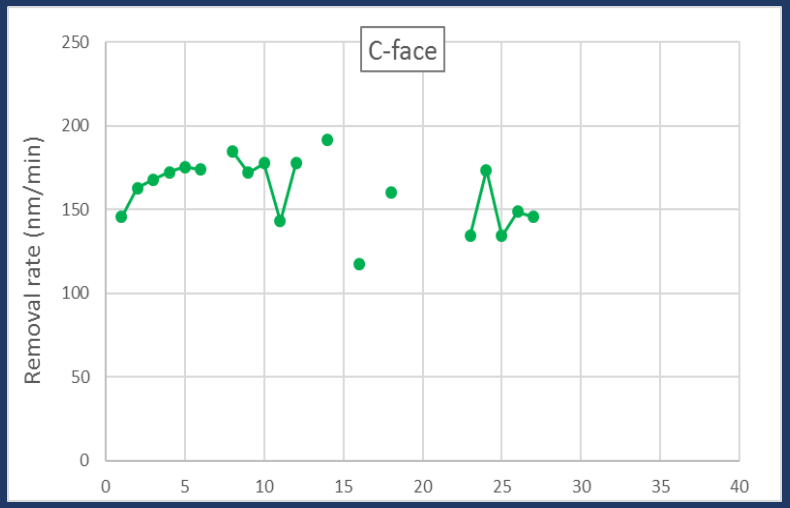
AFTER 360 nm

SiC processes

PRIMARY pad

SLURRY: SC-MC-HF2.0 (Sinmat)
PAD: Cabot D100 (primary)





RR = **124±35** nm/min

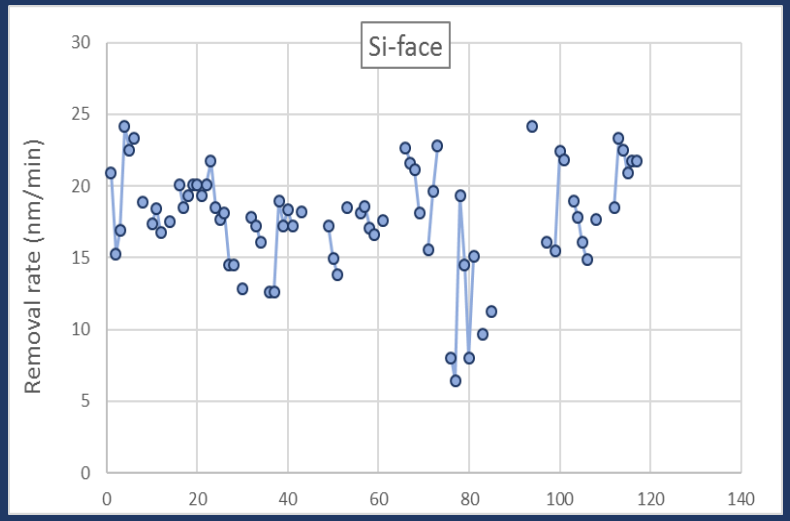
RR = **168±20** nm/min

- Removal rate is calculated from **weight** measurements
- It is affected by initial wafer **shape** and **surface structure**

Data given by ASCATRON

SiC processes

FINAL pad



SLURRY: SC1EN (Sinmat)
PAD: F TABLE 1 DOW (final)

RR = **17.7±4.2** nm/min

- Removal rate is calculated from weight measurements
- It is affected by initial wafer shape and surface structure
- Final table has **no conditioning pad**, resulting is wafer-to wafer change of polishing conditions

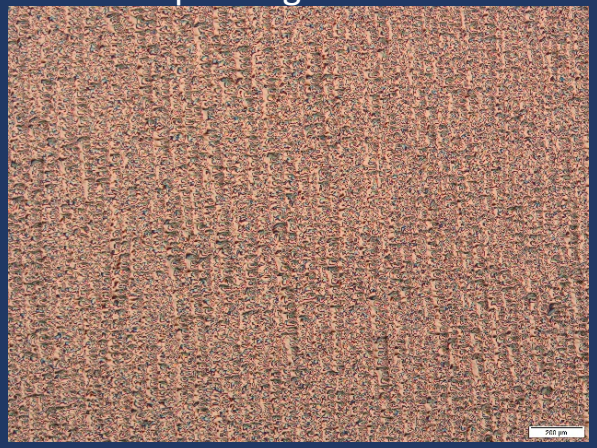
Data given by ASCATRON

CMP: post epi surface planarization

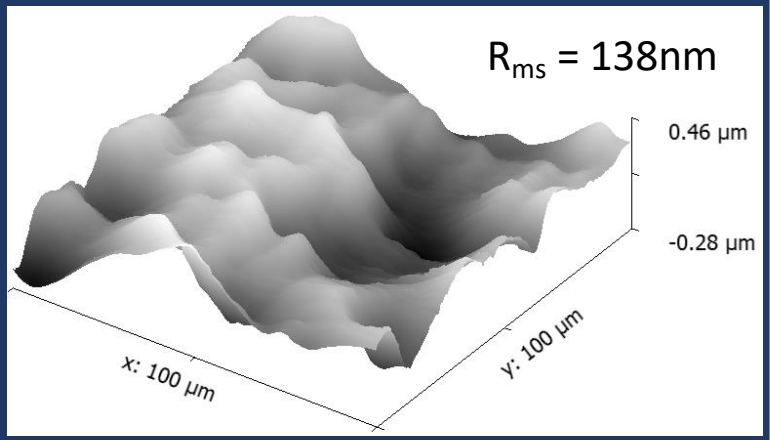
For **thick epilayers** (>30µm) surface degrades with a thickness due to step-bunching and defects

Typical surface after **260µm n-epi**

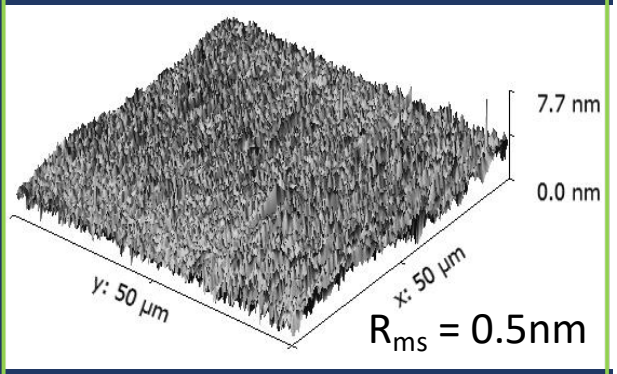
Microscope image



AFM



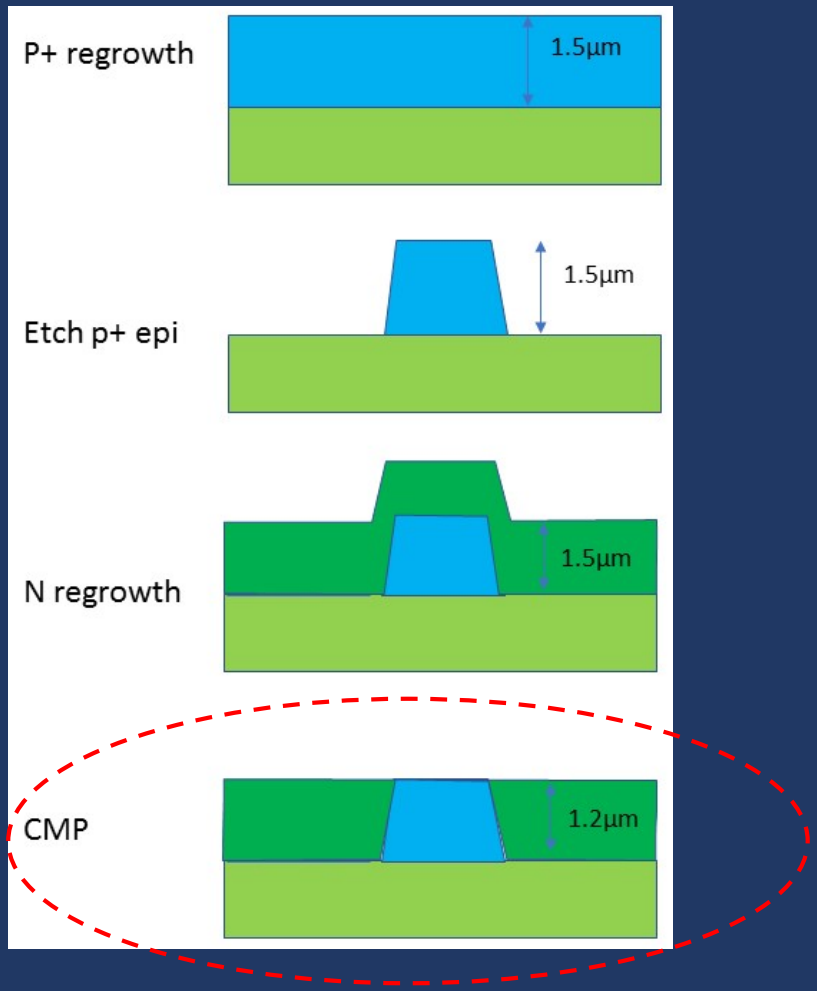
Surface after **CMP**



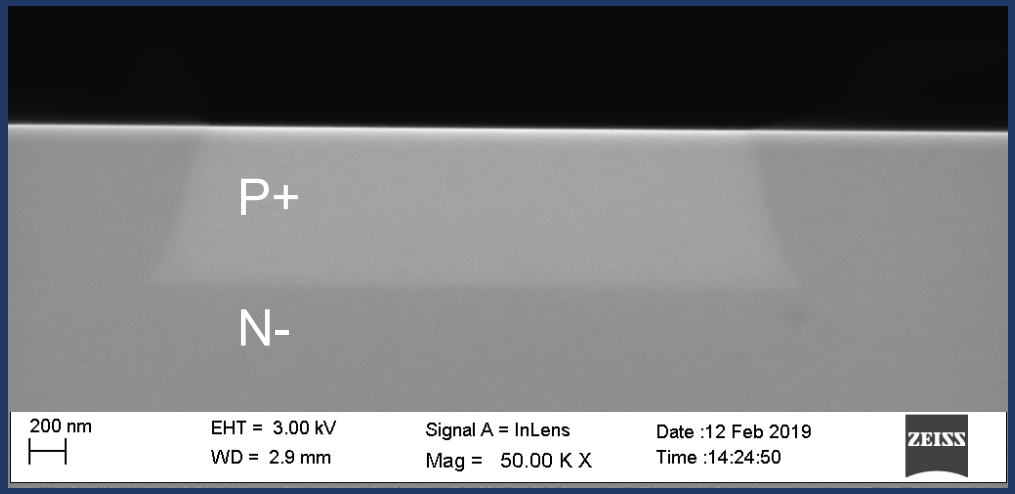
- Post epitaxial CMP planarization solves the problem of **surface degradation** and results in **epi-ready surface** with low Rms

Data given by ASCATRON

Processing of full-epitaxial 3DSiC® Structure



- Feasibility study of creating 3DSiC structures by combination of epi re-growth and CMP planarization
  - Epi growth of p+ layer
  - Formation of p+ islands by lithography and ICP etching
  - Epi re-growth of n-type layer
  - CMP planarization down to p+ islands
- Process successfully demonstrated



Data given by ASCATRON

Future development

- Full integration of **final pad** polishing for SiO_2/SiN processes
- Wafer **bonding** with GaAs/InP
- **Higher** level metalization processes

- **Metal** CMP (Tungsten plug)
- **3D** integration for CMOS

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What else is available in LIMS?

In VTT Aalto a Strasbaugh 6DS-SP CMP System is installed

- Dual polishing spindles for **100-200mm wafers**
- **Dual spindle** design provides for both single and double wafer processing, providing a significant throughput advantage
- **Hydrolift Load Station** improves loading reliability
- **Two table** design enables multi- step process capability
- **Pad conditioning** system provides in-situ programmable selective pad conditioning with 20 zones of programmable control

http://www.axustech.com/strasbaugh-6ds-sp-cmp-system

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Acknowledgment

- Joachim **Fritzsche** – for his work on SiN
- Mattias **Ekström** – for his work on metallization
- Axel **Strömberg** – for his work on GaAs/InP
- Linus **Vik** – for his work on SiC

Acknowledgment

- **Swedish Research Council** for the possibility of working on the project Fundamental Fluctuation in Spintronics (2017-04196).

- **Swedish Foundation for Strategic Research** for the possibility of working on the project CMPlab.

Thank you

MICRONOVA
Centre for Micro and Nanotechnology

myfab

NorFab
Norwegian Micro- and Nanofabrication Facility

DTU Danchip
National Center for Micro- and Nanofabrication

NNN
Nordic Nanolab Network