CMOS processing line for heterogenous integration at KTH

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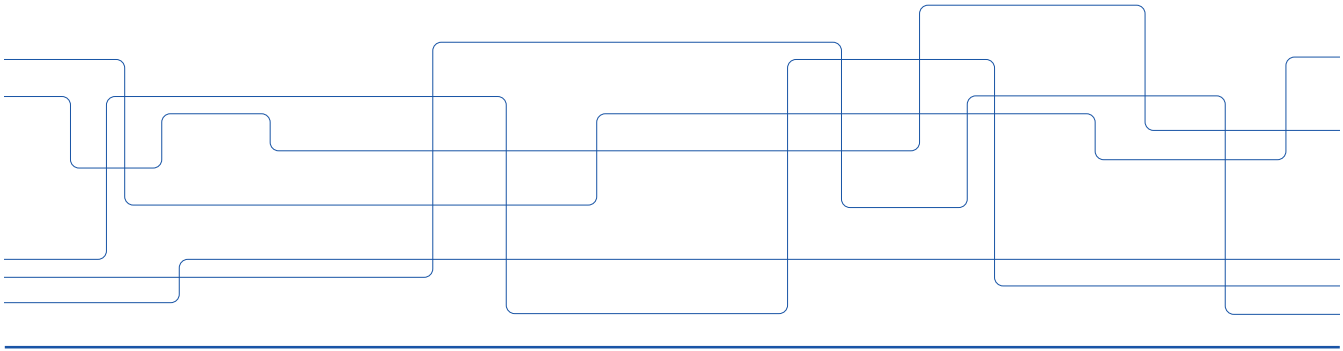
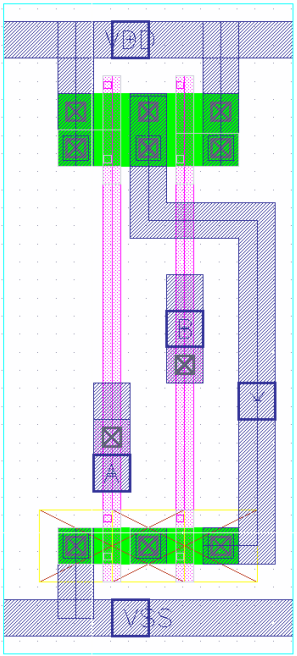
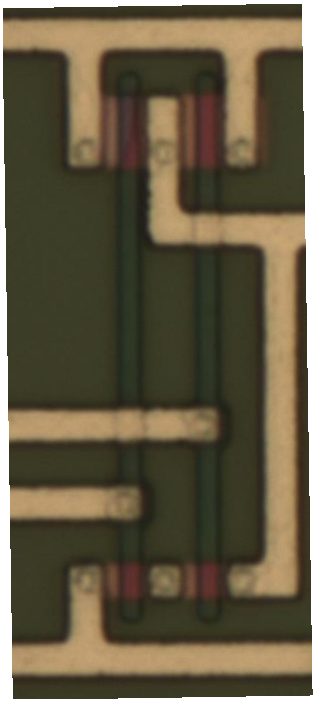


CMOS process line, why?

- Vision
  - Establish a CMOS process technology and design environment available to academic users
- Purpose
  - Benefit research where integration of electronic circuits would add value
- Current objectives:
  - Establish an in-house **reproducible and predictable** CMOS technology
  - Enable the technology in Cadence Virtuoso **design environment** used by circuit designers

Design Rules





I-line stepper, λ=365 nm

Resolution: 0.5 µm, Alignment: 50 nm

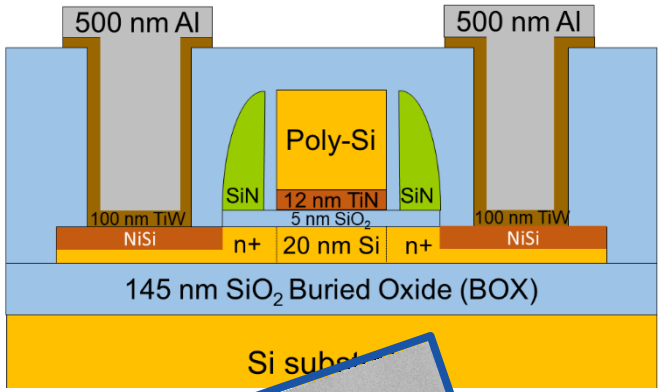
- Active area: width/open 2/2 µm
- Contact holes (CT): 1x1 µm^2
- M1, M2: width/open 2/2 µm
- M1-CT: overlap 0.5 µm
- L_G = 1 µm
- W_{PFET}=4 µm, W_{NFET}=2 µm

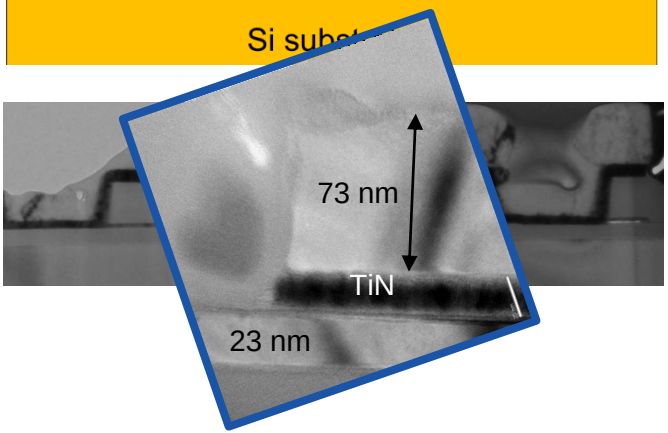
NAND: 16x36 µm^2

Die size of 7x7 mm : ~ 85 kNAND/die

Die size of 21x21 mm : ~ 765 kNAND/die

Fully Depleted SOI CMOS





1. **Alignment mark**
2. **Si device layer , t_{Si}=20 nm**

5 nm SiO_2 /12 nm TiN/100 nm n^+-poly-Si

3. **Gate mask and etch**
4. **n^+ As impl. 9 keV, 1e15 cm^{-2}**
5. **p^+ BF_2 impl. 9keV, 1e15 cm^{-2}**

ALD SiO_2/PECVD SiN spacers

RTA 1000 °C, 10s

6. **Silicide block mask**

NiSi formation

400 nm PECVD SiO_2

7. **Contact hole mask and etch**

100 nm TiW/500 nm Al

8. **Metal 1 mask and etch**

400 nm PECVD SiO_2

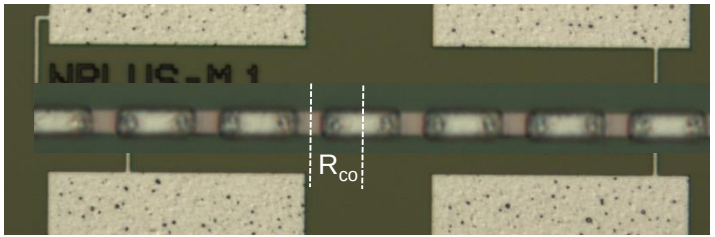
9. **Via hole mask and etch**

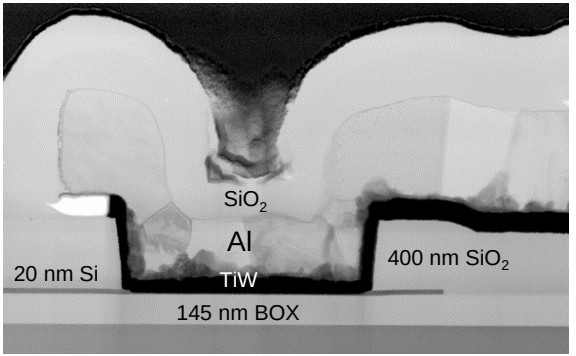
100 nm TiW/500 nm Al

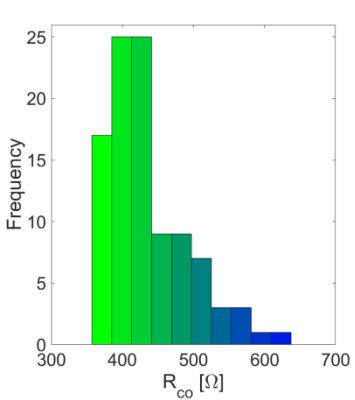
10. **Metal 2 mask and etch**

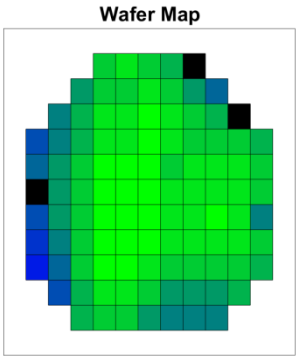
10 % H_2/N_2, 400 °C anneal

Contact chains



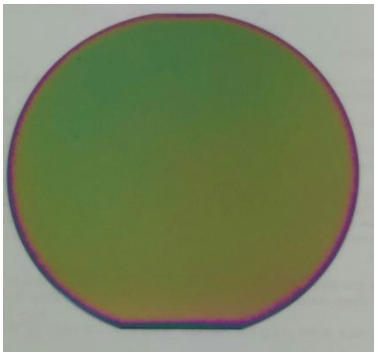


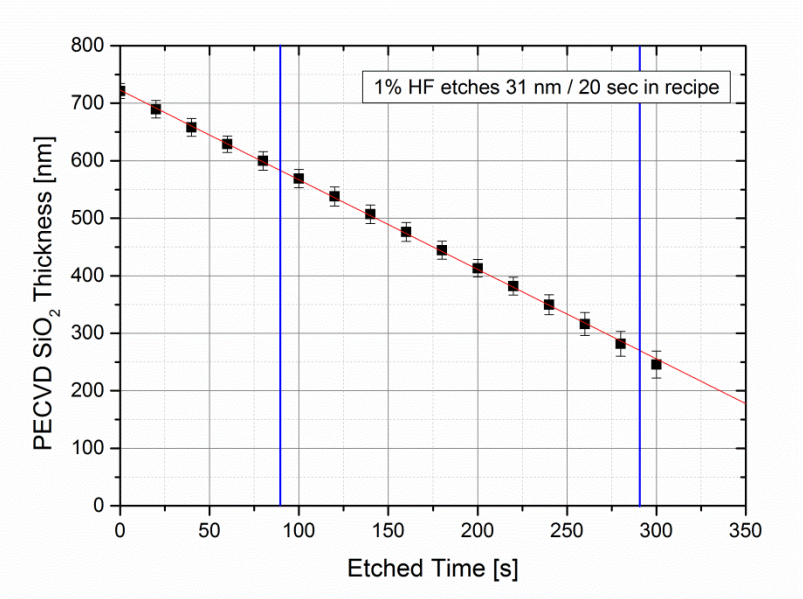




Contact process development	Yield [%]
ETCH: RIE to ENDP Resist strip: O_2 plasma DEP: TiW/Al	< 1%
ETCH: RIE to or close to ENDP Resist strip: O_2 plasma CLEAN: 1 % HF DEP: Ar^+ sputtering + TiW/Al	< 70%
ETCH: RIE on time *1 nm < t_{SiO2} < 40 nm left in CT hole* Resist strip: O_2 plasma CLEAN: 1 % HF 1 min DEP: TiW/Al	> 95 %

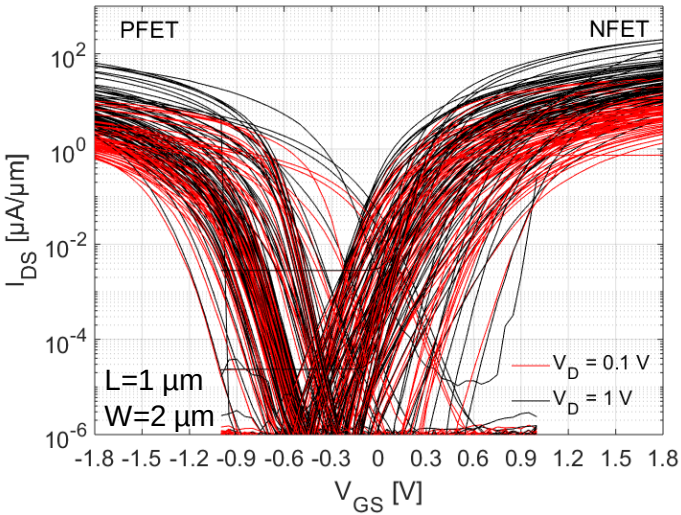
HF Spray etching

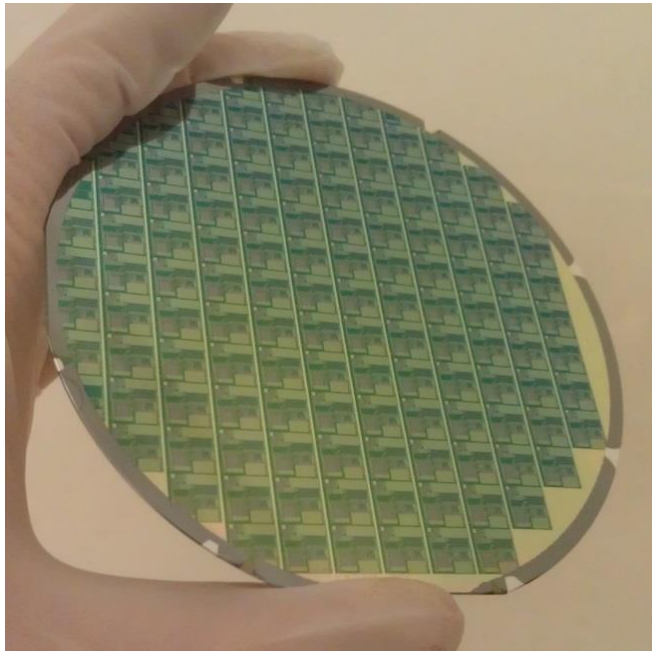




Process established Nov 2015

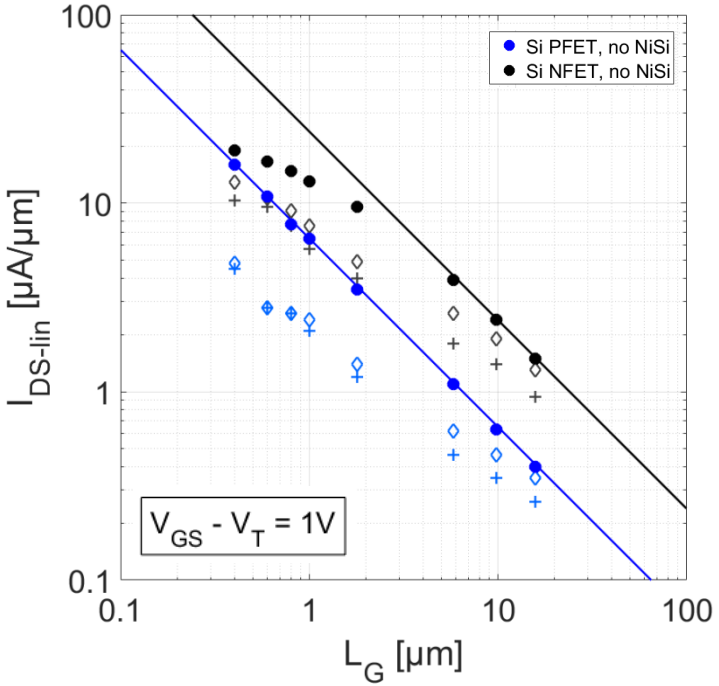
NFET and PFET electrical characteristics

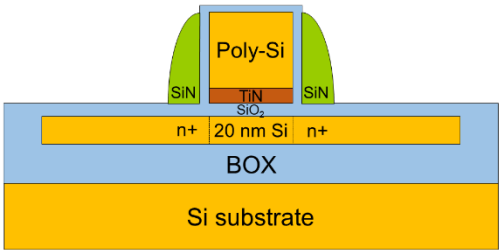




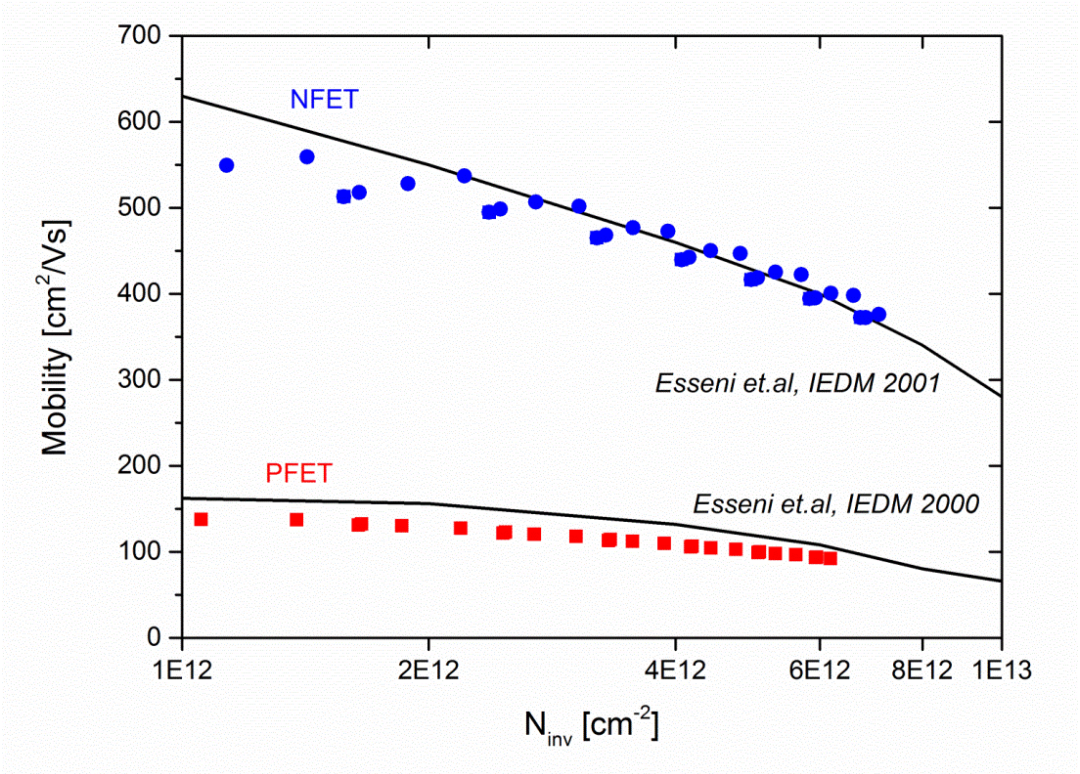
I_{DS} vs L_G

$$I_D = \mu C_{ox} \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}}{2}\right)V_{DS}$$

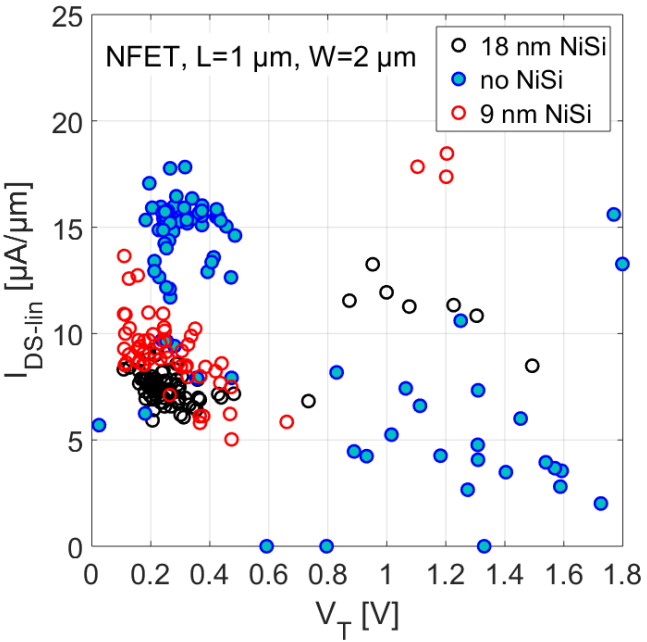


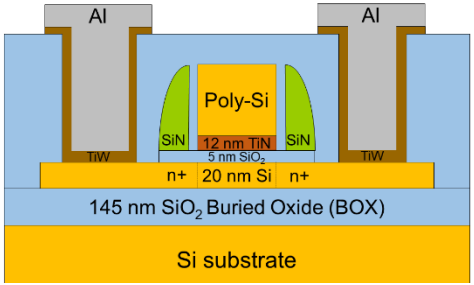


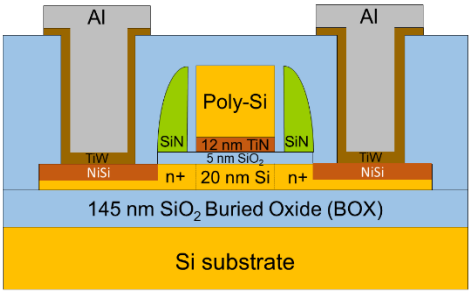
Long channel mobility



V_T variability

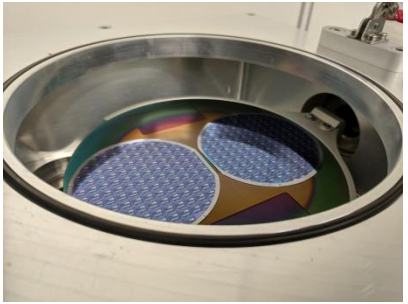


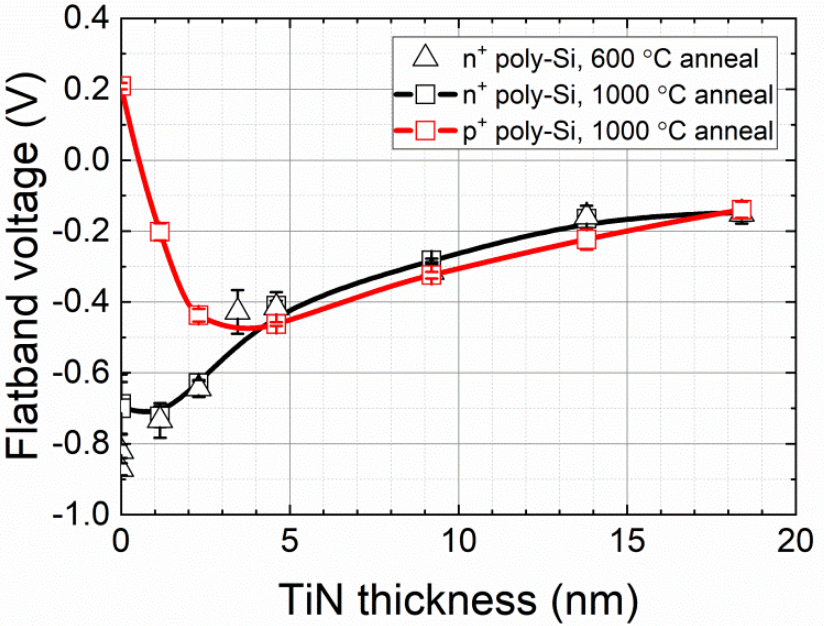




All devices have TiN deposited by PVD (magnetron sputtering).

ALD TiN, $TiCl_4$, NH_3, T_{dep}=425 °C

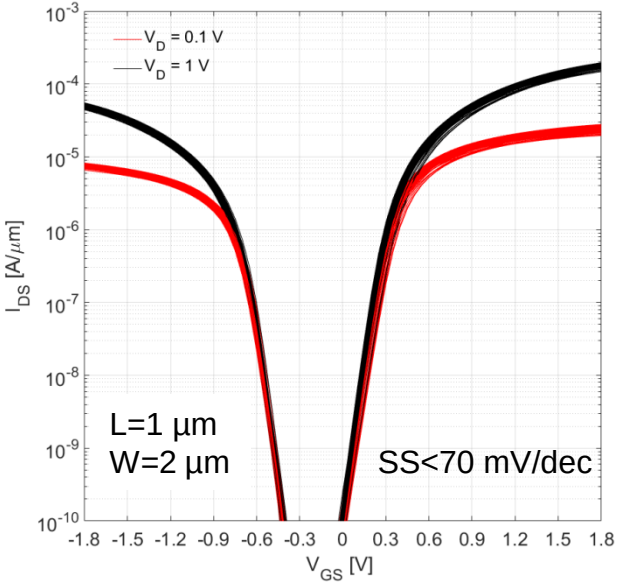


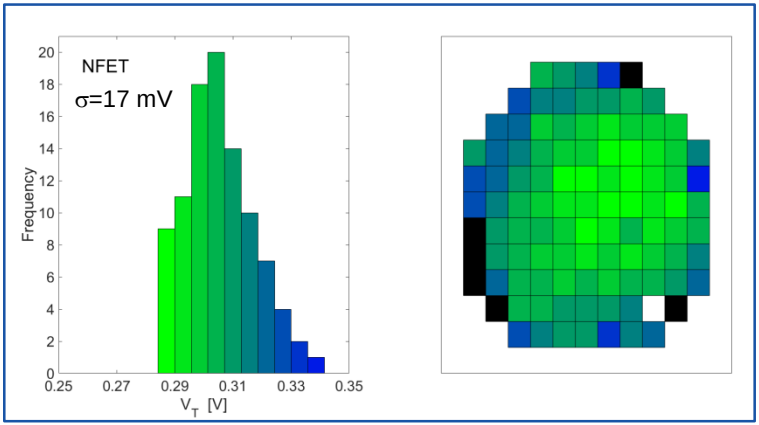


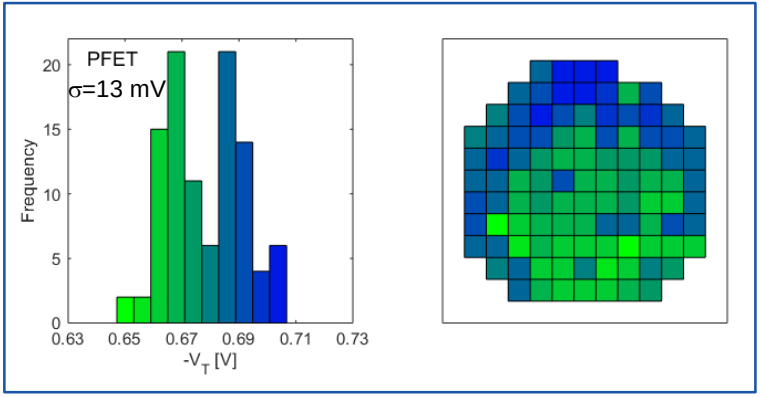
Summary CMOS Process Development

1. Contact hole etch and Metal 1 dep
2. No silicide
3. ALD TiN (T_{dep} = 425 °C) as gate electrode
4. Calibrate RTA, improved uniformity at T=1000 °C

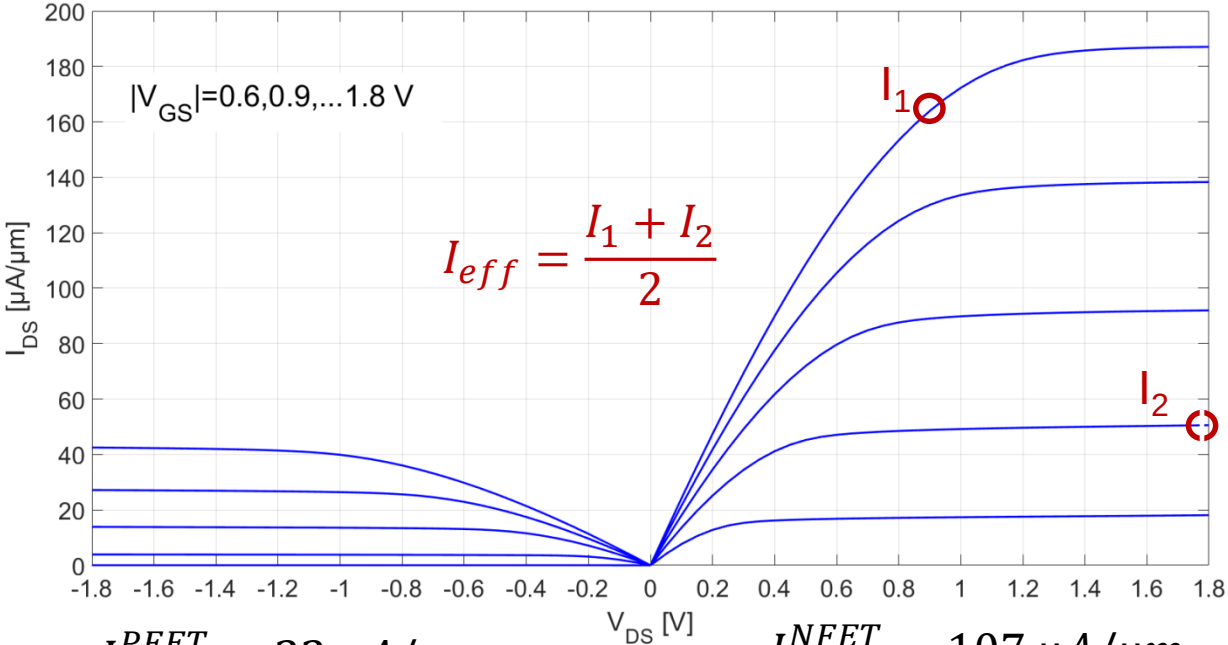
Device characteristics







Transfer characteristics



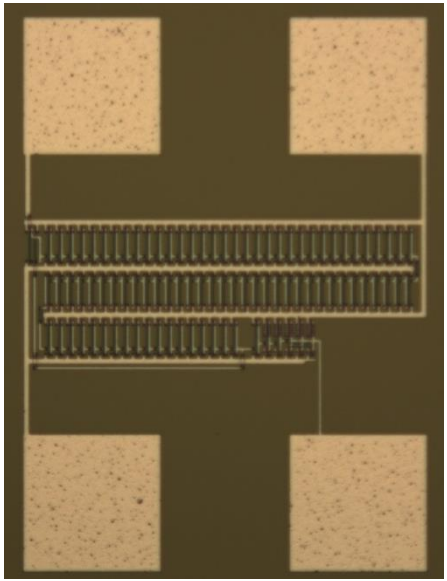
$$I_{eff}^{PFET} = 22\ \mu A/\mu m$$

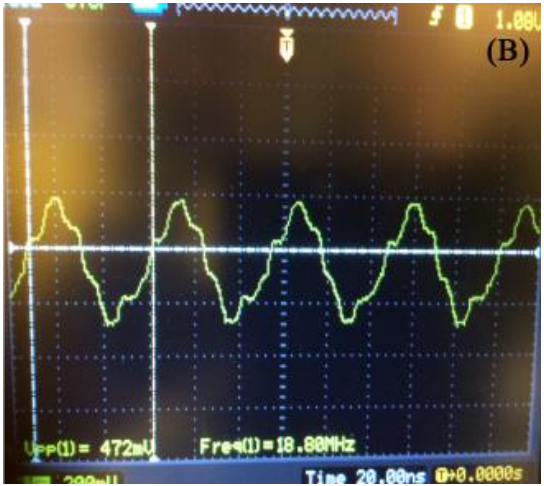
$$\tau_p = \frac{CV}{I_{eff}} = 565\ ps$$

$$I_{eff}^{NFET} = 107\ \mu A/\mu m$$

$$\tau_n = \frac{CV}{I_{eff}} = 116\ ps$$

87 stage Ring Oscillator (176 FETs)

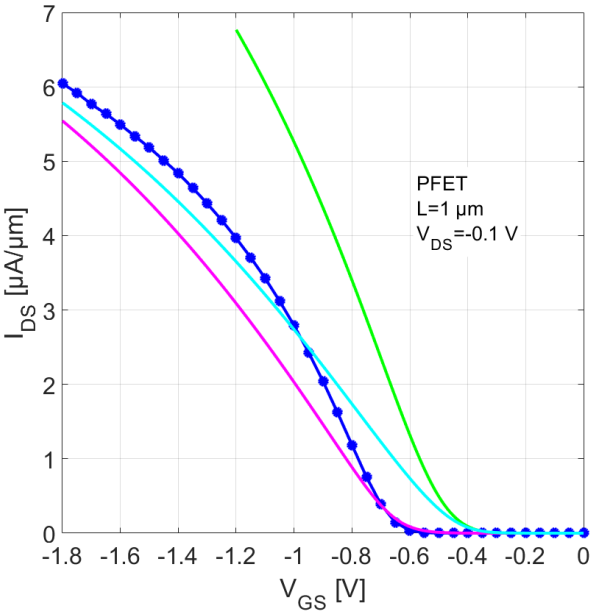


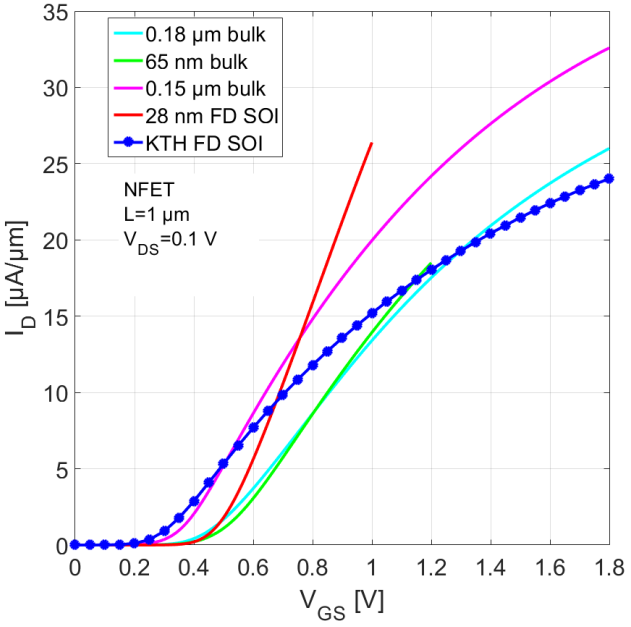


$$f_{RO} = 19\ MHz \rightarrow \tau = 305\ ps$$

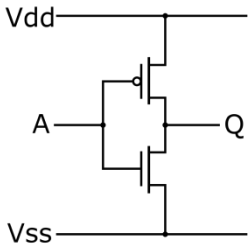
$$\tau = \frac{\tau_p + \tau_n}{2} = \frac{565 + 116}{2} = 340\ ps$$

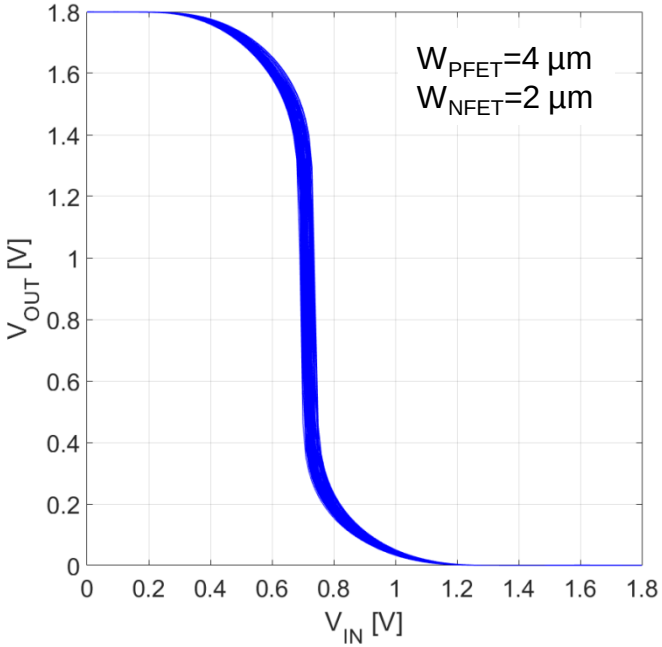
Comparision with commercial CMOS

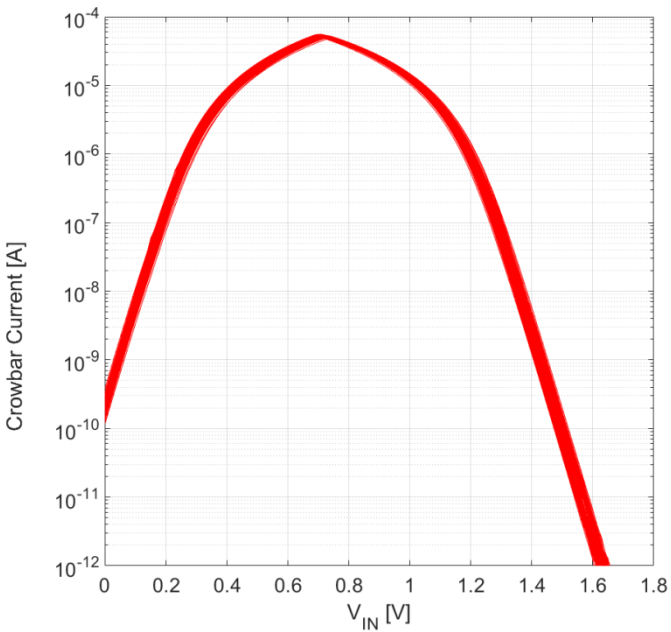




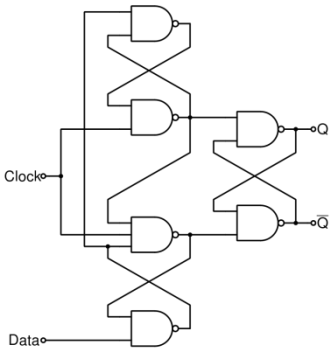
Inverter

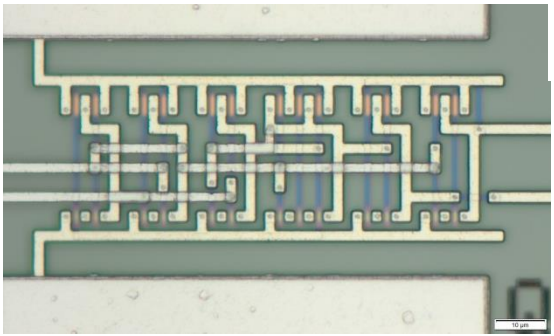

Vdd
A
Q
Vss

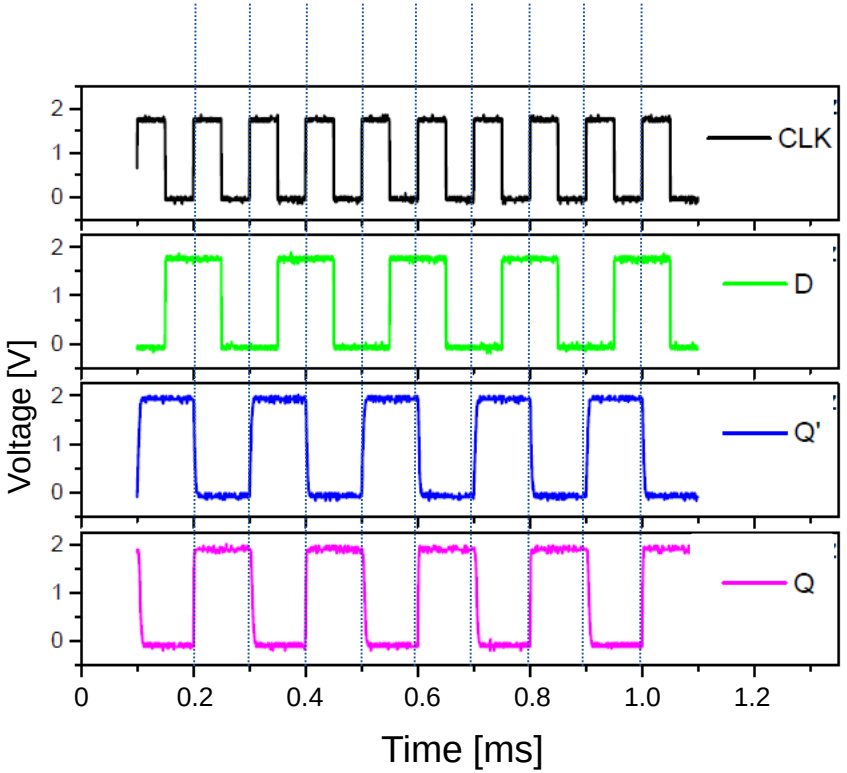

W_{PFET}=4 µm
W_{NFET}=2 µm
V_{OUT} [V]
V_{IN} [V]


Crowbar Current [A]
V_{IN} [V]

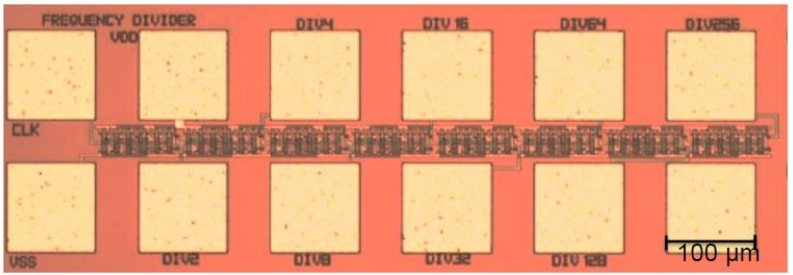
D-Flip-Flop (26 FETs)

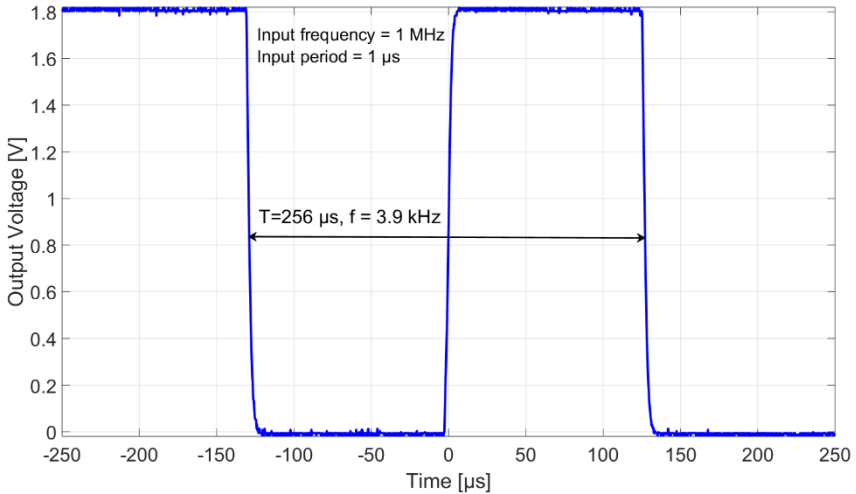






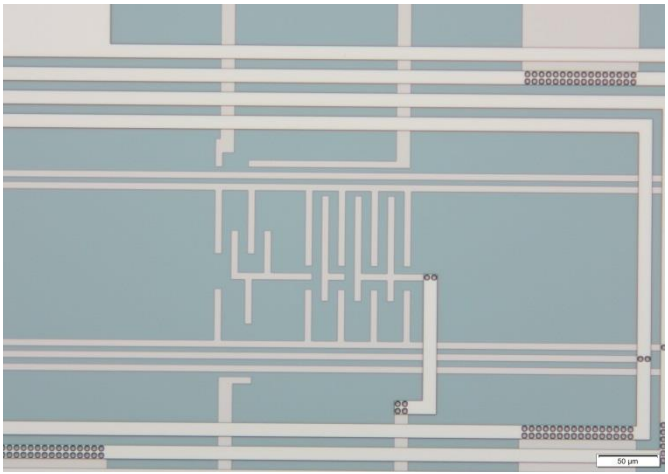
Frequency divider (8 DFF, 212 FETs)





FD SOI CMOS with M3

Oxide CMP based metallization



1. **Alignment mark**
2. **Si device layer , t_{Si}=20 nm**

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3. **Gate mask and etch**
4. **n^+ As impl. 9 keV, 1e15 cm^{-2}**
5. **p^+ BF_2 impl. 9keV, 1e15 cm^{-2}**

ALD SiO_2/PECVD SiN spacer

RTA 1000 °C, 10s

400 nm PECVD SiO_2

6. **Contact hole mask and etch**

Metal 1 deposition

7. **Metal 1 mask and etch**

PECVD SiO_2 + CMP

8. **Via1 hole mask and etch**

Metal 2 deposition

9. **Metal 2 mask and etch**

PECVD SiO_2 + CMP

10. **Via2 hole mask and etch**

Metal 3 deposition

11. **Metal 3 mask and etch**

PECVD SiO_2 + CMP

12. **Pad mask and etch**

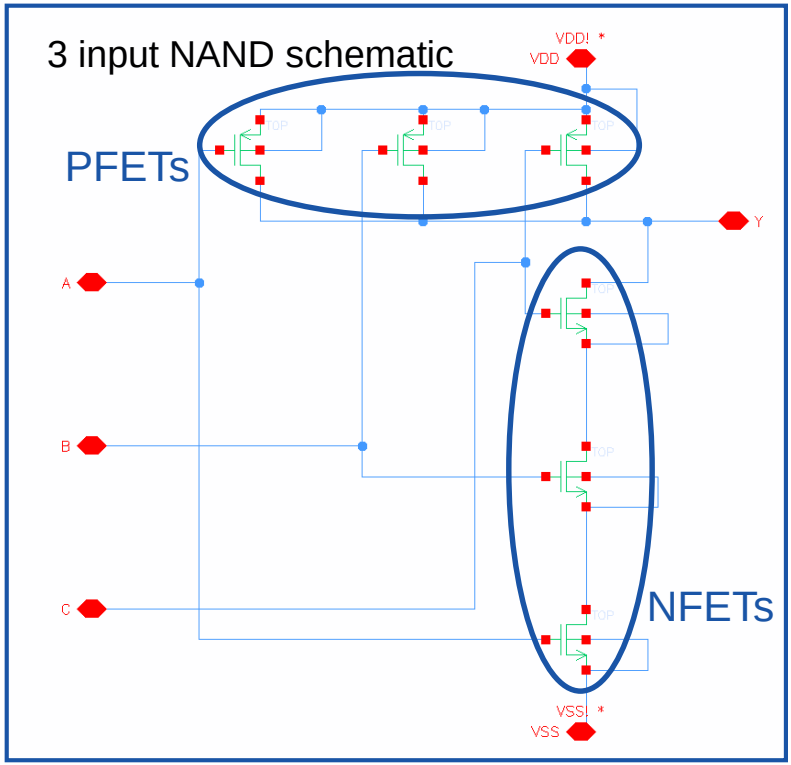
10 % H_2/N_2, 400 °C anneal

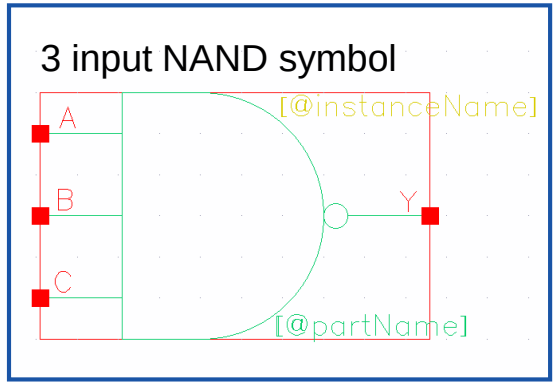
- Vision
  - Establish a CMOS process technology and design environment available to academic users

- Purpose
  - Benefit research and/or innovations where integration of electronic circuits would add value

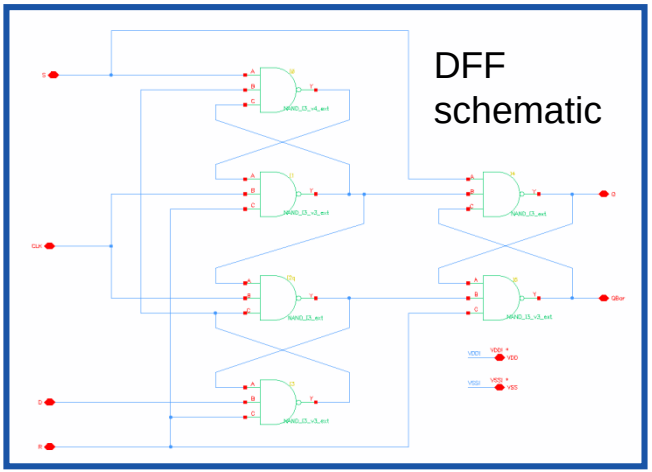
- Current objectives:
  - Establish an in-house **reproducible and predictable** CMOS technology
  - Enable the technology in Cadence Virtuoso **design environment** used by circuit designers

Design Environment





DFF with Set/Reset



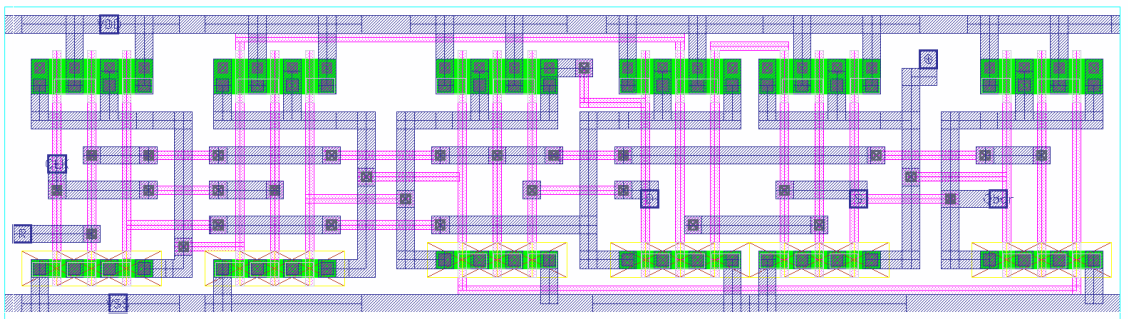
Design Rule Check (DRC)

Layout vs. Schematic (LVS)

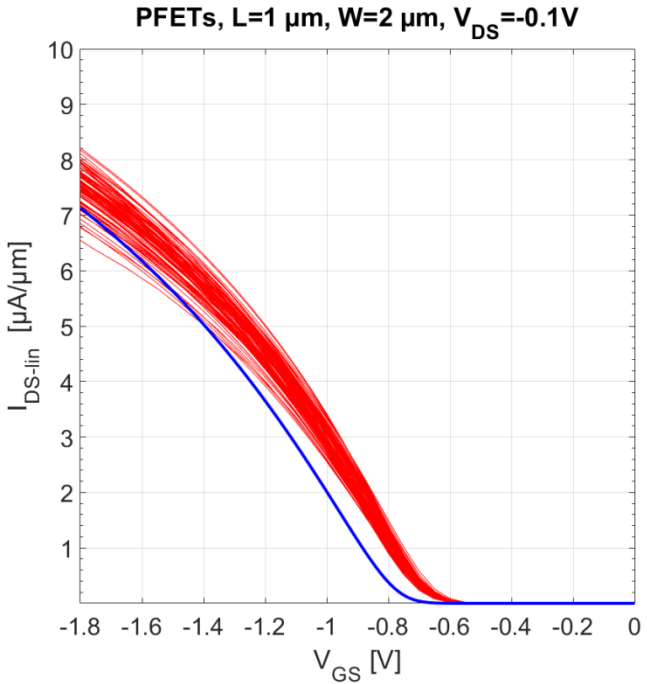
Process Design Kit (KTH FD SOI)

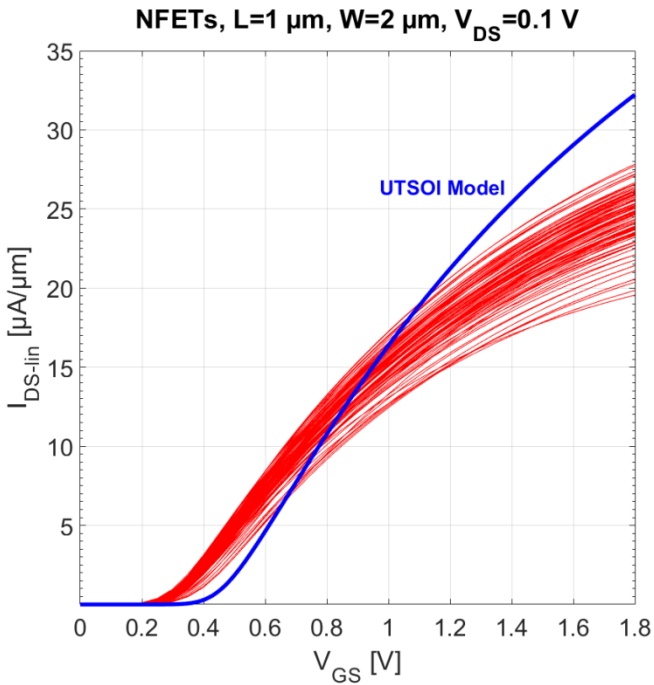
- Design rules (layers, min width, min distance….)
- Parametrisized MOSFETs
- Calibrated transistor model (UTSOI from Leti)
- Post layout extraction of parasitic R,C,L

DFF
layout



Calibrated UTSOI model (Leti)

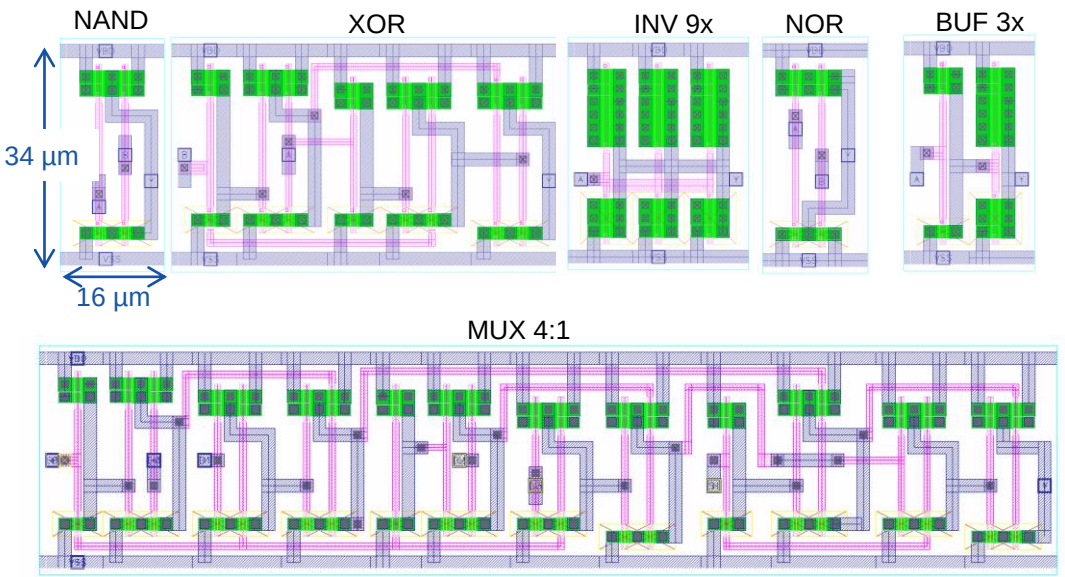




Model predicts 87-stage Ring Oscillator frequency of 22 MHz ($f_{meas.}$ = 15-19 MHz)

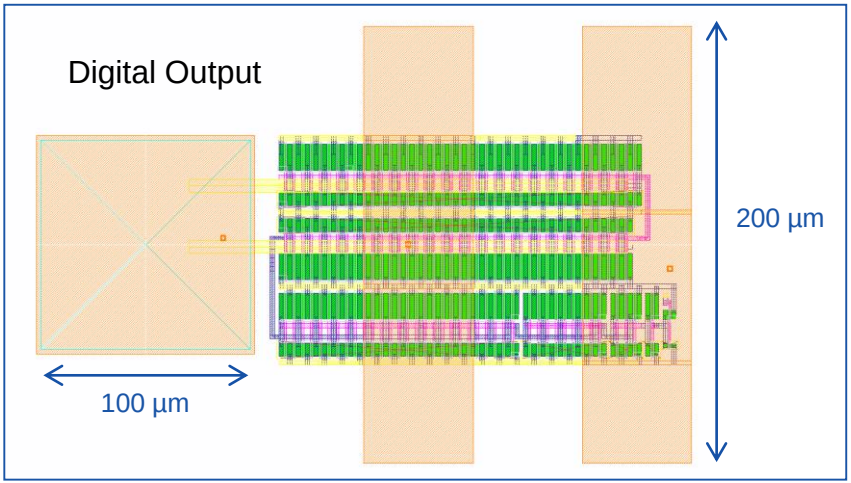
Digital Cell Library

Digital Cells
AND
NAND, 3NAND
OR
NOR
INV, INV_3x, INV_9x
XOR
BUF, BUF_3x, BUF_9x
BUF_TriState
MUX 2:1, MUX 4:1
DFF, DFF_SR



IO Cell Library

I/O Cells
Analog_IO
Analog_IO_ESD
Digital_Input
Digital_Input_ESD
Digital_Output
Digital_Output_ESD
VDD
VSS



Drive off chip capacitance=20 pF at t_{rise} ~ 1 ns

Work in progress….

- Adjust V_T of PFET and NFET +0.15 V to achieve symmetric V_T
- Reduce access resistance R_{SD} of NFET

- Improve calibration of UTSOI model
- Evaluate V_T variability of matched devices for analog circuits
- Evaluate antenna effect and incorporate rule in DRC
- Evaluate power consumption and timing

CMOS technology and circuits for heterogeneous integration

Goal:

- **establish a reliable CMOS technology** at KTH with necessary infrastructure to go from commonly used **Electronic Design Automation** environment to **fabricated wafers** in the myfab node **Electrum Laboratory.**

- provide academic **researchers** access to a **CMOS technology** that can be **adapted** to enable **integration with non-conventional devices** (e.g. biosensors, chemical sensors, energy harvester, optical components…) and thus enable research projects to exploit the benefits that on wafer integration with electronics can provide.

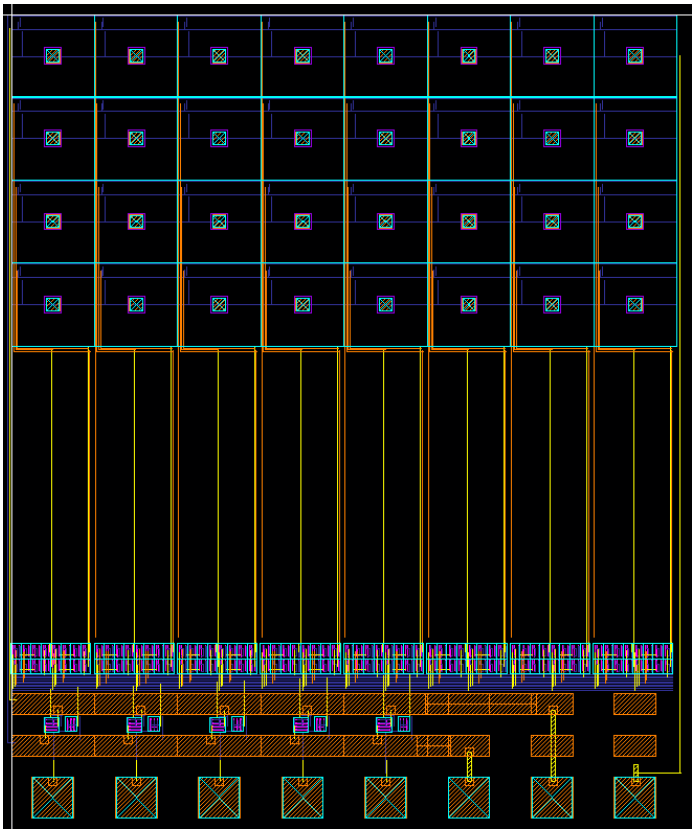
Project time: 2019-2021

Year 1: Establish technology and process design kit

Year 2 and 3: Collaborate with researchers and execute heterogenous integration with CMOS

Example: Chemical sensor

- 32 individul sensors
- 5 to 32 binary decoder
- Inkjet printing on sensor areas



Thanks to those who is doing the work….

Current and former PhD students








All M.Sc. students in the course Nanofabrication at KTH

Staff at Division of Electronics:



Staff at Electrum Laboratory

Thanks to those who is paying the work….

Vetenskapsrådet

myfab

Collaborate on heterogenous integration with CMOS?

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